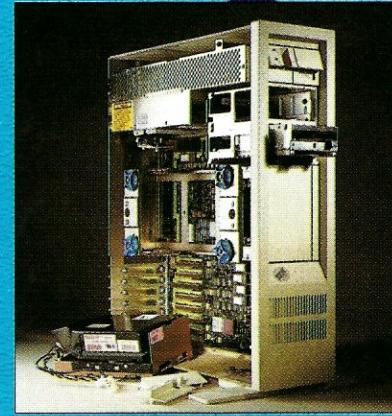
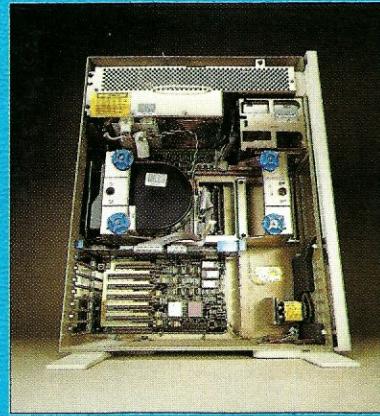
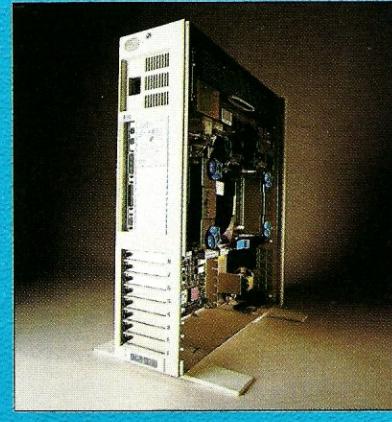
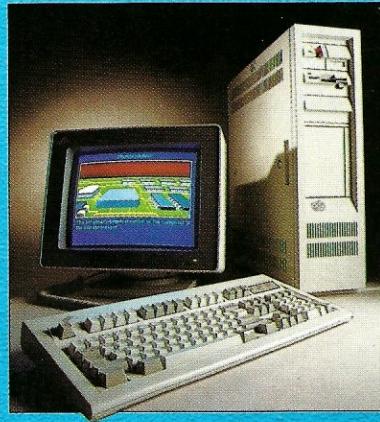


## Programming for Protected Mode Turbo Pascal

# Micro Systems

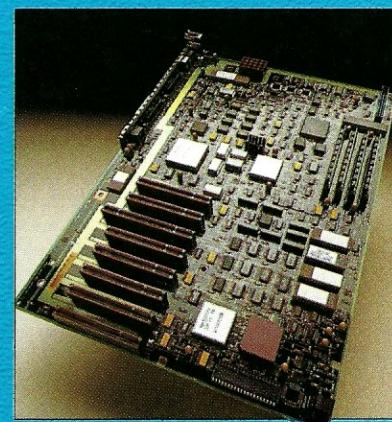
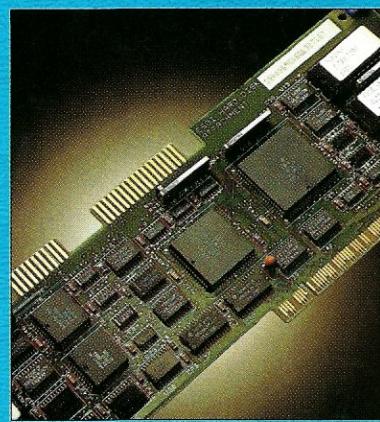
JOURNAL for the PC Systems Integrator

### George Morrow Looks Inside IBM's PS/2

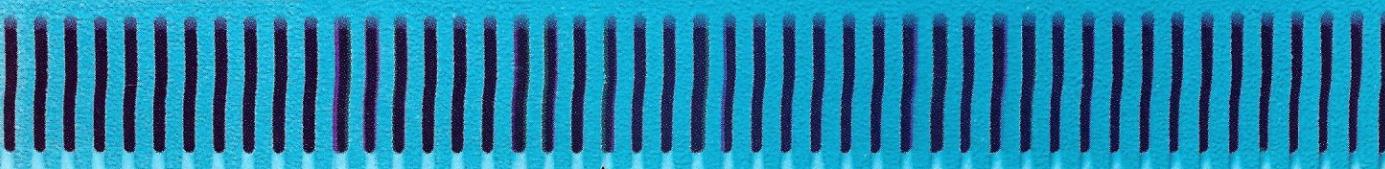


### Quadram's Low-cost LAN Solution

### Three XT Upgrades and DESQview Version 2.0 Reviewed



02



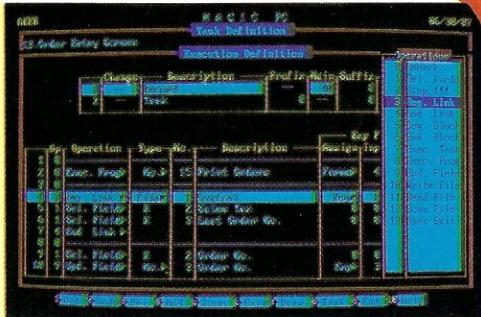
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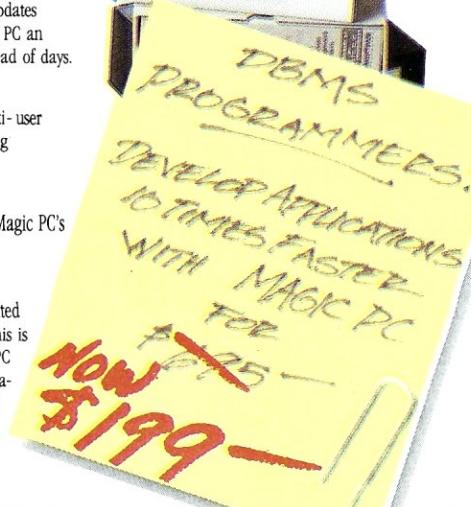
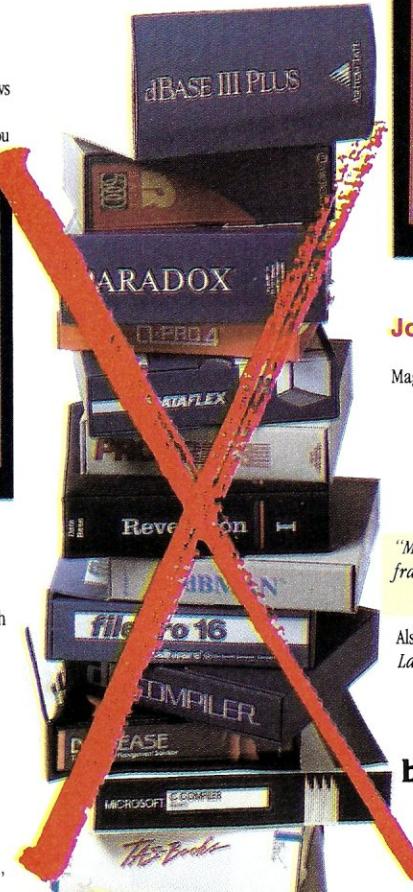
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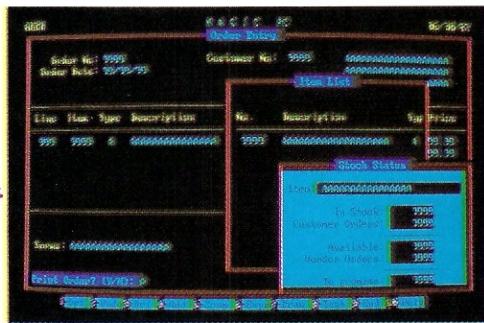
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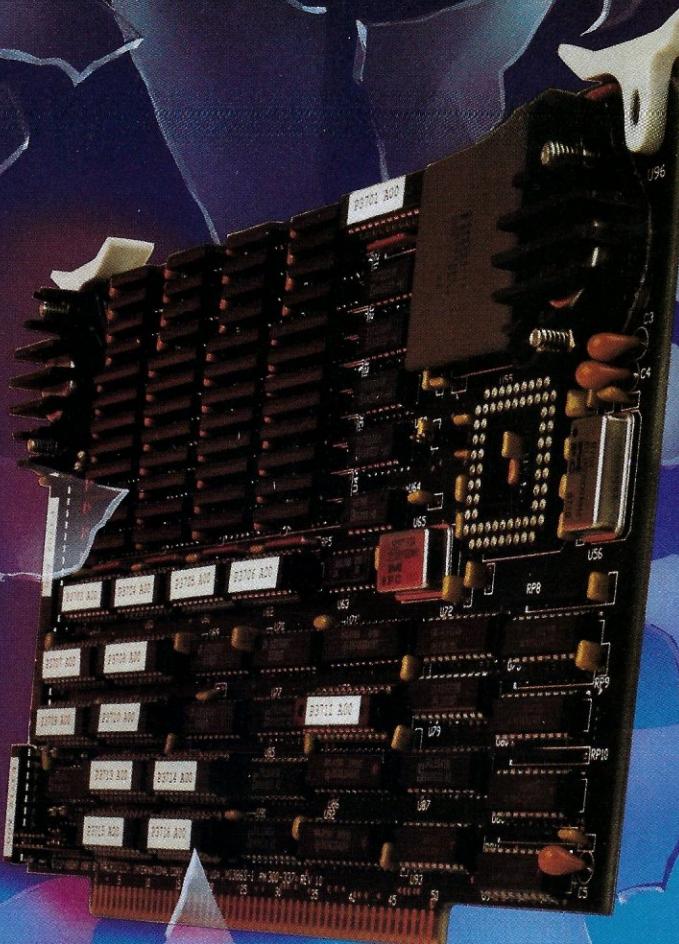
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# MicroSystems

JOURNAL for the PC Systems Integrator

February 1988

Vol. 4 No. 2

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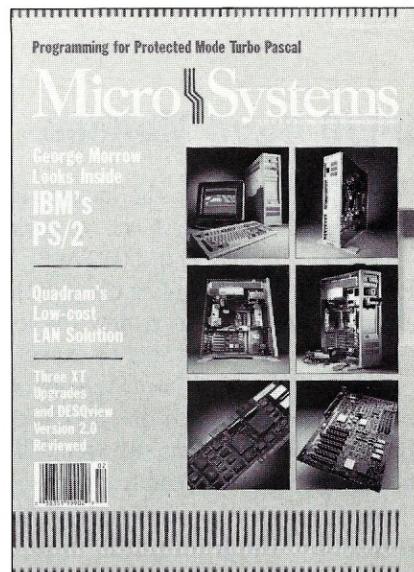
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**About the cover:** IBM's new PS/2 introduced a new bus architecture called the Micro Channel. Just as we have disassembled the IBM Model 60 on the cover of this month's *Micro/Systems*, George Morrow offers his own in-depth examination of this new bus, discussing some of its advantages and disadvantages, and providing the kind of structural insight required to interface to the Micro Channel. Our thanks to MicroAge Computer Stores, 1119 Industrial Road, San Carlos, Calif., for providing the equipment used on the cover.

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# From the Editor's Desk

by Sol Libes

## 9600-Baud Modems—Which Way To Go?

**W**ay back in the January/February and March/April 1987 issues of *Micro/Systems*, we reviewed five 9600-baud modems: the Electronic Vaults UPTA96, Racal Vadic 9600VP, Telebit Trailblazer RA12E-T1, U.S. Robotics Courier HST, and Codex 2260. We currently have a project underway to review the lower-cost 9600-baud modems that have since been introduced and we expect to publish this review soon.

The editors of *Micro/Systems* are heavy users of modem communications—sending files to one another and downloading and uploading files to Bulletin Board Systems. We would like to send and receive our messages and files as quickly as we can to cut transmission time and connect-time costs.

But more than a year has gone by and we have not upgraded our modem technology. The primary reasons are the high cost of 9600-baud modems and, worst still, the lack of compatibility. While the costs have come down somewhat, the compatibility problem is still there. To communicate at 9600 baud, you currently must have the same manufacturer's modem as the system with which you are communicating.

Since we spend a great deal of our communication time on Bulletin Board Systems, we have watched very carefully for a trend in 9600-baud modems among BBS sysops. I recently surveyed more than 1,000 PC-based Bulletin Board Systems and, to my surprise, I discovered 303 systems already are using 9600-baud modems.

Of those 303 BBS systems, I counted 219 (72.3 percent) using the USR 9600-baud modem, 42 (13 percent) using the FastComm modem, 34 (11.2 percent) using the Microcom 9600-baud modem, 5 (1.75 percent) using the Telebit modem, and 3 (0.99 percent) using the Hayes 9600-baud modem. USR's popularity is no doubt due to the fact that USR offered BBS sysops a \$500 discount very early on, dropping the modem price from \$995 list down to \$495. FastComm and Microcom followed with similar sysop offers. Hayes is a late entrant into this market and is only just now offering a sysop special.

USR appears to be setting the 9600-baud standard. And there are rumors that some 9600-baud modem makers will provide upgrades to a 9600 standard when it is established. At the recent Comdex show, Multi-Tech Systems and Telenetics Corporation introduced 9600-baud modems that are compatible with the Microcom modem, indicating a compatibility concern among modem manufacturers. In the meantime, we have decided to wait just a little while longer before moving up to 9600 baud.

Sol Libes

Continued on page 6

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JOURNAL for the PC Systems Integrator

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# News & Views

## Random Gossip & Rumors

Microsoft is hard at work on the next version of DOS. Look for a possible release in the late spring. It should provide a new user interface, hard disk storage greater than 32 megabytes, and built-in EMS 4.0 support.

Microsoft's new product, an attempt to win away Borland software devotees, is rumored to be a Turbo Pascal-to-Quick C converter program. Word is that Microsoft is considering putting the program in the public domain.

IBM has shown a PS/2 Model 90 to selected customers and dealers. The Model 90 contains 20-MHz 386 and RT-like RISC processors, 4 megabytes (MB) of RAM, and high-speed video systems.

Don't expect to see much in the way of OS/2 application software until next year. Most software houses are waiting for the release of the Presentation Manager (PM) before getting down to serious OS/2 applications development work, and IBM and Microsoft do not expect to release the PM until the fall. At this point, the OS/2 software arena looks like a place where only the major software houses will compete. However, Microsoft is expected to release a low-cost OS/2 development kit to encourage small software developers to introduce applications.

Later this year, Sony, Sharp, and Verbatim are expected to introduce high-capacity, removable, rewritable, optical disk drives that may challenge Winchester hard disks as primary storage devices. Sony's drive is expected to store 650 MB, have a 120-millisecond access time, use an SCSI interface, and cost about \$1,000.

## 1987—The Year of the AT

It is estimated that 3.5 million AT-compatible machines were shipped last year. This made the AT the

most popular category of personal computers. And even stronger unit sales are expected this year as 286 clock speeds increase and many 386 machines also start to use the basic AT architecture.

Most of last year's 286-based systems ran at 8-10 MHz. This year the more popular 286 AT-compatibles are expected to have 12-16 MHz clocks, with a few running at 20 MHz. The AT architecture is also being modified so that more of the processor's memory is on a fast local bus while only I/O controller cards are on the slower AT bus.

## Chip Capacity Going Up

Toshiba, which currently ships about 50 percent of the one-megabit RAMs, has begun sampling four-megabit RAM chips with production promised for the third quarter. Texas Instrument, Mitsubishi, and Matsushita will begin shipping samples soon, with production scheduled to begin late in the last quarter or first quarter of next year. Hitachi, Fujitsu, NEC, IBM, and Siemens have also announced that they will introduce 4-Mb memory chips. This means that we can begin to see these chips appearing in desktop systems some time next year.

## Interesting IBM Tidbits

Is there such a thing as an IBM standard operating system? The U.S. government's General Services Administration (GSA) conducted a survey recently and found that there is indeed one operating system that runs on all current IBM systems—UNIX! The U.S. government has been attempting to establish standards for purchases of computer hardware and software. The survey was conducted in an effort to establish a standard operating system for government computers.

While IBM lists its entire PS/2 line as desktop systems, one must note that the Models 60 and 80 are too big to fit on a desktop and are designed to sit on the floor.

According to the *Wall Street Journal*, IBM dropped from first to second place in 1987 in the *Jour-*

*nal's* list of the world's largest public companies. They were replaced by NTT of Japan. AT&T dropped from 5th to 17th, while DEC rose from 72nd to 36th. Eight of the 10 largest companies are now Japanese-owned, compared to five the previous year.

## More Interesting IBM Info

IBM has reportedly shipped close to 2 million PS/2 systems in the 10 months since their introduction. By contrast, it took then about four years to reach that same quantity with the PC systems. Most of the PS/2 systems shipped have been the low-end Models 25 and 30, which are essentially upgraded XT machines. IBM is now cranking out about 10,000 PS/2s daily from plants in Boca Raton, Florida; Raleigh, North Carolina; Austin, Texas; and three European sites.

William Lowe, President of IBM's Entry Systems Division, revealed that IBM developed the latest version of PC-DOS (Version 3.3) and licensed it to Microsoft.

IBM also has announced that AIX (IBM's UNIX for the PS/2) will be shipped in September. In addition, they announced that the technical specs and programmer's tool kit for Version 1.1 of OS/2 will be shipped in October.

## Atari Demos Powerful Workstation

Atari stunned Comdex attendees with a workstation system based on the Inmos transputer operating at 10 mips (million instructions per second) or 1.5 mflops (million floating-point operations per second). Atari claimed that a more powerful system could be assembled with four transputer cards to provide 130 mips, or about 19.5 Mflops. Atari also announced that it was developing a  $1280 \times 960$  display. The system uses a UNIX-like operating system that supports X-Windows, GEM, Fortran, and several development languages.

Atari also announced that it will introduce a 68030-based system later this spring. It will be a multiuser system running Whitesmith's Idris operating system. §

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## Testing FORTRAN Compilers

*Dear editor:*

I found Tetewsky and Feenberg's review of "FORTRAN Compilers for the PC" (September/October 1987) interesting. However, I would like to know how they determined what an "i-stand" extension is. A more commonly used term is VAX FORTRAN compatibility. One extremely useful extension is the use of certain obviously constant expressions freely in the context of constants, e.g.,

```
PARAMETER (BELL=CHAR(7),  
           SR2=SQRT(2.),  
           ASCZRO=ICHAR('0'))
```

which is not permitted by many compilers.

It seems impossible to find a compiler validation test that addresses issues which are more significant in practice than whether one can GO TO an END IF or use ASSIGN. Some of these issues are covered clearly by the standard, but others are not. Certain compilers reject such obvious code as

```
WRITE(*,*)(X)
```

or READ and WRITE files unsymmetrically. All compilers accept the SAVE keyword (equivalent to static in C), but some ignore it, even though they use what are called auto variables in C. Some compilers treat

APPEND as the default, possibly so that they can get that effect without using an "extension" keyword. Many compilers interpret UNKNOWN in unusual manners. It should not be absolutely necessary to use keywords not defined in the ANSI standard, such as CARRIAGE CONTROL. Compilers differ in the precision of evaluation of expressions involving constants, and the ability to control this by defining PARAMETER constants is frustrated by the rejection of the sort of expressions given above. DEC compilers still have restrictions on identifiers used in statement functions (macros to C coders) which have been removed even in IBM compilers.

An "i-stand" trend which should not be encouraged is the requirement of non-standard source code for efficient operation. In the older versions of VAX FORTRAN with which I was familiar BYTE arrays were preferred, although the same code could be made to run much more slowly with CHARACTER arrays. The programmer had to control register allocation by using new names for each intended instance of a register variable and possibly inserting redundant operations outside a loop to prevent others from being allocated to registers.

Tim Prince  
American Institute of  
Aeronautics & Astronautics  
Walled Lake, Michigan

## Ordering Floating Point Operations in C

*Dear editor:*

Don Libes' discussion of floating point operations in his "C Forum" column ("Double Trouble," September/October 1987) was very informative. However, I would like to make two points concerning the order of floating point operations.

First, using the example values of  $x = 1.0E8$ ,  $y = -1.0E8$ , and  $z = 1.0$  causes loss of precision only on storage in an architecture that uses 8-byte doubles. That is the reason that

```
float temp,x,y,z;
```

```
x = 1.0E8;  
y = -1.0E8;  
z = 1.0;  
temp = y + z;  
temp = temp + x;  
printf("Sum = %g\n", temp);  
temp = (x + y) + z;  
printf("Sum = %g\n", temp);
```

produces the results Sum=0 and Sum=1 is not due to the order of evaluation, but rather due to the loss of precision when  $y + z$  is stored into temp. A correct example of the effects of order evaluation is the following:

```
double float temp,x,y,z;  
  
x = 1.0E20;  
y = -1.0E20;  
z = 1.0; temp = y + z;  
temp = temp + x;  
printf("Sum = %g\n", temp);  
temp = (x + y) + z;  
printf("Sum = %g\n", temp);
```

The second point is that there is a portable method of forcing a different order of evaluation that should work with all K&R compliant compilers. It is based on the fact that a cast has the same precedence as a unary operator. Thus, the following example will produce the results Sum = 1 and Sum = 0, respectively:

```
double temp,x,y,z;
```

```
x = 1.0E20;  
y = -1.0E20;  
z = 1.0; temp = ((double)  
(x + y)) + z;  
printf("Sum = %g\n", temp);  
temp = x + (double)(y +  
z);  
printf("Sum = %g\n", temp);
```

Ed Hannon  
St. Petersburg, Florida

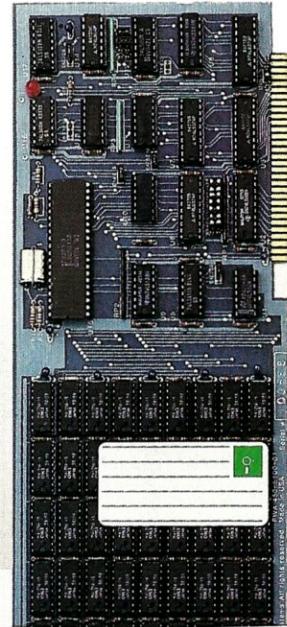
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# Dump from the hip

*This column features tips and techniques for using the C language productively. It discusses typical problems encountered in using C, and offers solutions. Reader suggestions, comments, and questions are encouraged and can be addressed to: "The C Forum," Micro/Systems Journal, Box 1192, Mountainside, NJ 07092.*

This month's column presents a useful debugging tool—a dump routine (Listing 1). While rather mundane in function, its implementation illustrates several things:

- 1) It is possible to treat memory like a file (or "stream").
- 2) It is possible to pass functions as parameters.
- 3) It is possible to package code in such a way that it can be called from a program, a debugger, or run standalone.

As a program, dump is invoked as "dump filename." The contents of the file are listed in hex and ASCII side by side. Each line of 16 bytes is preceded by its offset from the beginning of the file. Figure 1 shows

**Figure 1. The beginning of a typical dump file**

```
0: 54 68 69 73 20 6d 6f 6e 74 68 27 73 20 63 6f 6c
10: 75 6d 6e 20 70 72 65 73 65 6e 74 73 20 61 20 75
20: 73 65 66 75 6e 20 64 65 62 75 67 69 6e 67 20
30: 74 6f 6f 6c 20 2d 20 61 20 64 75 6d 70 20 72 6f
40: 75 74 69 6e 65 2e a 57 61 6e 69 6c 65 20 72 61 74
50: 68 65 72 20 6d 75 6e 64 61 6e 65 20 69 6e 20 66
60: 75 6e 63 74 69 6f 6e 2c 20 74 68 65 20 69 6d 70
```

the beginning of this column, run through dump.

dump may be called from a program as follows:

```
dump(address, length, outfile);
```

"Address" is the address of memory at which to start dumping. "Length" is how many bytes should be dumped. "outfile" is a file for output, so that we can study the results later.

Notice that the dump program doesn't take the same arguments as the dump subroutine. For example, the dump program doesn't require an output file because we can assume the output can be redirected by the (UNIX) shell or the (DOS) command processor. The other differences between the arguments should be obvious.

By using "#ifdef MAIN", it is possible to generate both the stand-alone program and the dump subroutine from the same source. When MAIN is defined, main() is created, otherwise dump() is created. Both main() and dump() call a function that does the real work of dumping, real\_dump().

Consider the problem of writing real\_dump(). The formatting part is simple enough, but where does the input come from? getchar() is the solution for reading in the file, but when real\_dump() is called as a subroutine, it needs to get input directly from memory. Similarly, we could pass the address and a length to real\_

dump() but that wouldn't work for files.

One solution is to define two different dump routines, but that is somewhat annoying since so much of the code is the same. A cleaner solution is to pass an input routine to real\_dump()—whenever it needs the next byte, the routine simply calls the input routine. The input routine passed by main() will return the next character from the file while the input routine passed by dump() will return the next character from memory.

Here is the input routine for main():

```
int file_input()
{
    return(getchar());
}
```

The input routine for dump() is only a little more complicated.

```
int
mem_reader()
{
    if (count++ = length)
        return(EOF);
    else
        return((int)*address++);
}
```

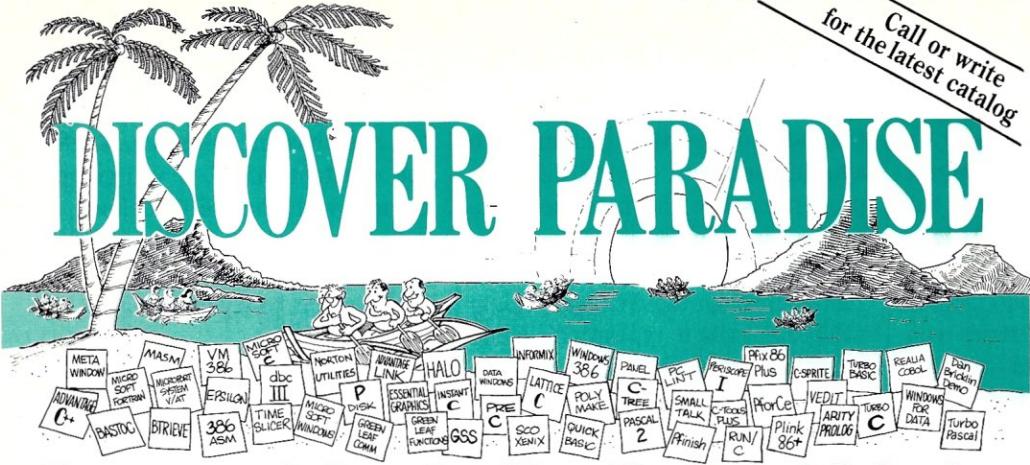
Three global variables set by dump() allow mem\_reader() to appear as if it is reading from a stream. In particular, when we have read "length" bytes, EOF is returned, otherwise we simply return the character at the next address.

Notice that each of these routines returns an *int*, rather than a *char*. This is to allow passing EOF to terminate the input. Now we have enough to declare real\_dump():

```
real_dump(address, infunc, ofp)
char *address;
int (*infunc)();
FILE *ofp;
```

Here, *infunc* is declared as "a pointer to a function returning an *int*." Inside real\_dump(), the line where we use *infunc* looks like:

```
... = (*infunc)();
```



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The last argument of *real\_dump()*, *ofp*, is a FILE pointer that is presumed to be opened by the caller, in this case either *main()* or *dump()*. *main()* simply passes *stdout*, but *dump()* requires some elaborate coding.

The problem that *dump()* faces is that some debuggers restrict you from passing literal strings as arguments to procedure calls. The C compiler normally places literal strings in the initialized data space of a program. After linking it may be

impossible to increase this space. Therefore, the debugger is left with the choice of inserting the literal into another segment having different properties than the initialized data space, or not doing it at all.

To avoid the problems of passing strings through the debugger, *dump* will prompt you to type in a file name if *outfile* == 0. Supplying a null file name (" ") will send the output to *stdout*.

To create *dump()*, you need to create an object file that you can link

to. Simply compile *dump.c* with no change. To compile *dump.c* and create a standalone program, #define the constant *MAIN*. If you compile *dump.c* with the *TEST* defined, an executable will be produced along with the subroutine *dump()*, and a variable, *foo*, to try dumping. §

*Don Libes is a computer scientist working in the Washington, D.C., area. He works on artificial intelligence in robot control systems.*

**Listing 1. A dump routine for debugging**

```
/* dump.c - dump from file or memory
Author: Don Libes
Date: October 1, 1987
*/
#include <stdio.h>
#include <ctype.h>
#define ROWLENGTH 16
#ifndef MAIN
static FILE *ifp; /* shared between main and file_reader */
int
file_reader()
{
    return(getc(ifp));
}
main(argc,argv)
int argc;
char **argv;
{
    if (argc != 2) {
        printf('usage: dump file\n');
        exit(1);
    }
    if (!(ifp = fopen(argv[1], 'r'))) {
        perror(argv[1]);
        exit(1);
    }
    real_dump((char *)0, file_reader, stdout);
}
#else
static int length; /* shared between dump() and
mem_reader() */
static char *address; /* ditto */
static int count; /* ditto */
int
mem_reader()
{
    if (count++ >= length) return(EOF);
    else return((int)*address++);
}
dump(address_parm,length_parm,outfile)
char *address_parm;
int length_parm;
char *outfile;
{
    char outfilebuffer[80];
    FILE *ofp;
    if (!outfile) {

```

```
        printf('output file (<cr> for stdout): ');
        gets(outfilebuffer);
        outfile = outfilebuffer;
    }

    if (*outfile) {
        if (!(ofp = fopen(outfile, 'w'))) {
            perror(outfile);
            exit(1);
        }
        else ofp = stdout;
    }

    count = 0;
    length = length_parm;
    address = address_parm;

    real_dump(address,mem_reader,ofp);
    if (outfile && *outfile) fclose(ofp);
}

#endif

real_dump(address,infuc,ofp)
char *address;
int (*infuc)();
FILE *ofp;
{
    int i, row[ROWLENGTH];

    while (1) {
        for (i=0;i<ROWLENGTH;i++)
            row[i] = (*infuc)();
        if (row[0] == EOF) break;

        /* first print address */
        fprintf(ofp, '%4x: ', address);
        /* then print hex */
        for (i=0;i<ROWLENGTH;i++)
            fprintf(ofp, (row[i] != EOF) ? '%2x ':' ',row[i]);

        /* lastly print characters */
        fprintf(ofp, ' ');
        for (i=0; i<ROWLENGTH; i++) {
            if (row[i] == EOF) break;
            if (isprint(row[i])) putc(row[i],ofp);
            else putc('. ',ofp);
        }
        putc('\n',ofp);
        address += ROWLENGTH;
    }
}

#endif TEST
/* here is something to dump, as well as containing a file
to dump to */
char foo[] = {'f', 'o', 'o', 0x0, 0x10, 'a', 'b', 0x18, 0xff,
0, 0x4};

main()
{
}
#endif
```

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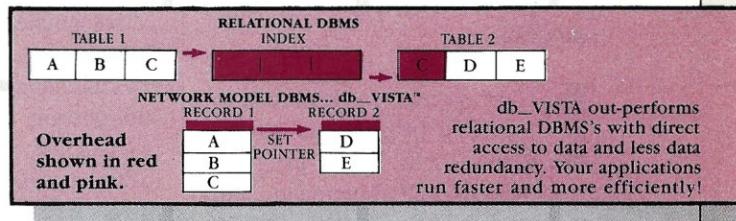
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by Stephen R. Davis

## Disassembling Turbo and Using INLINE to Debug (Part 2)

*This column features tips and techniques for productively using Turbo Pascal on MS-DOS and PC-DOS microcomputer systems. Reader suggestions, comments, and questions are encouraged and can be addressed to: Turbo Pascal Corner, Route 5, Box 107L, Greenville, TX 75401; or through MCI mail, 289-6124.*

Last month we discussed including breakpoints directly into Turbo Pascal programs using the INLINE command. This month we will take that concept one step further, but first we should take another quick look at the Turbo Pascal horizon.

### Disassembling Turbo Pascal

Roughly a year ago, I became aware of a disassembler for Turbo Pascal offered by C. C. Software. This product accepts as input the Turbo Pascal compiler and generates commented assembler source code as its output. No module headings are included, and getting oriented within the source code is pretty difficult at first. However, there are sufficient comments that the reader can eventually figure it out.

The idea of having access to the source code for Turbo Pascal is

pretty exciting. With such a program one can change Turbo to match custom requirements. Do you need a version of Turbo to generate ROMable code? How about a subset of Turbo running outside of DOS? Want to modify the run-time library? All these things and more can be performed by the experienced programmer who has access to the source code.

There was only one problem. At the time, C. C. Software only offered a disassembler for the Z80 version of Turbo Pascal, and the number of users still using Z80 machines is small and getting smaller. I was disappointed, but I asked C. C. Software to stay in touch. Recently they called me back to tell me they now have a disassembler for PC-DOS Turbo!

The new disassembler package takes Turbo Pascal Version 3.01a non-8087 and generates 10 assembler source files. These resulting source files are in a slightly peculiar but readable format. They are adequately commented and they have some module headings. C. C. Software includes an assembler that assembles and relinks the separate source files back together again.

To test the package, I disassembled my own TURBO.COM. The process is laborious but straightforward, and took a little less than an hour. Reassembling the 10 source files again was very quick, but resulted in a .COM file that was not identical to

the original. I was not surprised when a few of the instructions did not match exactly. There are a few instructions on the 8086 that can be coded in one of two different ways—which way your assembler chooses is immaterial. I was a little concerned, however, when the newly created .COM file was some 4 bytes longer than the original.

With an impending sense of doom, I executed the "new" Turbo compiler. I was relieved to discover, however, that the new compiler operated exactly like the original without any apparent bugs being introduced.

The source code listings generated by C. C. Software's disassembler is not trivial. You are not going to be able to sit down and master the inner workings of the Turbo Pascal compiler in one evening. C. C.'s manual does provide some guidance as to where and how the various functional blocks operate, and with enough perseverance any experienced assembler programmer should be able to understand it all.

In the meantime, C. C. Software makes some interesting suggestions to improve program performance under Turbo 3.0: (1) Avoid passing sets as arguments to procedures since there is a bug in this code under certain conditions; (2) Due to a bug in the compiler, the DO after a WHILE is optional; (3) Avoid using the standard string and set operations because they are very slow; and (4) Always code floating point constants with the decimal point to avoid conversion at run time.

C. C. Software is located at 1907 Alvarado Ave., Walnut Creek, CA 94596; (415) 939-8153. The Turbo Pascal disassembler is available for \$67.50 and they do accept credit card phone orders. Also available from C. C. Software are several CP/M-80 disassembler packages. Call for a catalog.

### Turbo Pascal 4.0

Of course, C. C. Software's work may be rendered less important by the introduction of Turbo Pascal 4.0. As this is written, I have just received a late beta version for review.

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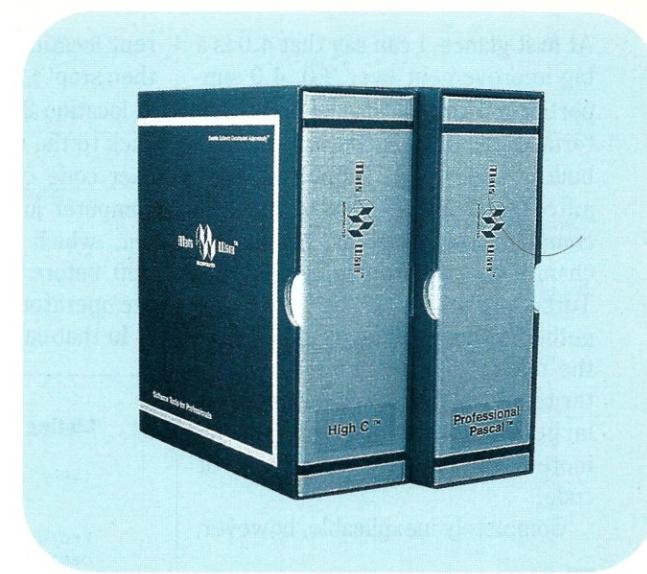
Computer Language	February 1986, '87
Dr. Dobb's Journal	August 1986
PC Magazine	Jan. 27, 1987 (80386 version)
Dr. Dobb's Journal	July 1987 (80386 version)
BYTE Magazine	November 1987 (80386 version)

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## The Clear Choice for Large Programming Projects

— PC Tech J.

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At first glance, I can say that 4.0 is a big improvement over 3.0. 4.0 supports the now standard Borland interface. Included in the package is a built-in Link facility supported by an automatic Make—no more recompiling the entire project just to change one procedure. In addition, Turbo 4.0 can now be linked together with other languages. In fact, the manual devotes an entire chapter to the subject. Added support for large memory models means no more 64K limit on either data or code.

Completely inexplicable, however,

## When executing TURBO.COM under DEBUG, INLINE statements stop execution of the Pascal program at predetermined key points.

is that a debugger is still missing from the Turbo environment of 4.0. True, a load map can be generated from the link step so that "load map" debuggers, such as Symdeb, Periscope, and PFix, can be used, however, executing one of these debuggers means leaving the Turbo environment. Hopefully, this shortcoming will be solved by third parties as well as it was in Turbo 3.0. I will be using 4.0 on my next programming project for this column and will report further when it is completed.

### Today's Topic

Last month I discussed using the INLINE statement to generate breakpoints directly in Turbo Pascal source code. In that column I demonstrated how debuggers uniformly use the interrupt instructions, INT 1 and INT 3, to generate breakpoints. If, for example, I enter the command G 200 from within DOS' DEBUG (meaning "continue from the cur-

rent location up to location 200 and then stop"), DEBUG places an INT 3 at location 200 before giving control back to the user program. When the user code executes the INT 3, the computer jumps back to the debugger, which then restores location 200 before displaying a prompt to the operator.

In that earlier column, I also dem-

onstrated how the INT 1 breakpoint instruction could be included directly into our Pascal source code using INLINE (\$CD/\$01) statement. When executing TURBO.COM under DEBUG, these INLINE statements stop execution of the Pascal program at predetermined key points. When combined with a basic knowledge of DEBUG and assembly language pro-

#### **Listing 1. Initiate Single Step using \$U under DEBUG 3.x**

```
{SetSingleStep - patch DEBUG 3.0 so that INT 3 functions
  identically to INT 1. Tested under DOS 3.0 and
  3.1}
Procedure SetSingleStep;
begin
  {$U-}
  inline ($CD/$01);      {break to debugger}

  inline ($06/          {push es}
        $31/$DB/        {xor bx,bx}
        $8E/$C3/        {mov es,bx}
        $26/$C4/$1E/$0C/$00/ {es:les bx,[c]}
        $B8/$90/$90/    {mov ax,9090}
        $26/$89/$47/$03/ {es:mov 3[bx],ax}
        $26/$89/$47/$05/ {es:mov 5[bx],ax}
        $07            {pop es}
      )
end;

var
  i: integer;

begin
  setsinglestep;      {initialize INT 3}
  {$U+}
  for i := 0 to 10 do
    writeln ('sample loop #', i)
  {$U-}
end.
```

#### **Listing 2. Same routine designed for DOS 2.1 DEBUG**

```
Procedure SetSingleStep_2_1;
begin
  {$U-}
  inline ($CD/$01);      {break to debugger}

  inline ($06/          {push es}
        $31/$DB/        {xor bx,bx}
        $8E/$C3/        {mov es,bx}
        $26/$C4/$1E/$0C/$00/ {es:les bx,[c]}
        $B8/$90/$90/    {mov ax,9090}
        $26/$89/$47/$02/ {es:mov 2[bx],ax}
        $26/$88/$47/$04/ {es:mov 4[bx],al}
        $07            {pop es}
      )
end;
```

#### **Listing 3. Sample output while single stepping sample prc**

```
-g
sample loop #0

AX=FF00 BX=00B7 CX=000A DX=A433 SP=FFFC BP=FFFE SI=284F DI=0166
DS=41FD ES=41FD SS=9000 CS=3F6E IP=28AA NV UP EI PL NZ NA P O NC
3F6E:28AA E85AF7    CALL  2007
-g
sample loop #1

AX=FF00 BX=00B7 CX=0009 DX=A434 SP=FFFC BP=FFFE SI=284F DI=0166
DS=41FD ES=41FD SS=9000 CS=3F6E IP=28AA NV UP EI PL NZ NA P O NC
3F6E:28AA E85AF7    CALL  2007
```

gramming, this technique becomes a potent debugging tool. (Without going into great detail, the two breakpoint interrupts are equivalent, except that the INT 1 stops on the next machine instruction while the INT 3 stops on the current one).

This is a powerful technique for examining smaller sections of code, including manually examining large numbers of **INLINE** statements. However, it can become quite a job in a program of any size, and yet this is exactly what is needed to "single-step" individual Turbo Pascal statements. As it turns out, Turbo Pascal can be induced to automatically include breakpoint instructions.

The compiler directive **\$U** is described on Page 315 of the Version 3 Turbo manual as the "user interrupt" directive. The manual explains that setting this directive allows the program to respond to a Ctrl-Break at any time. Although not obvious from the manual's short description, Turbo does this by adding an INT 3 at the beginning of the code generated for each Pascal statement. At startup, Turbo initializes INT 3 to a small section of code within the Turbo library that checks the keyboard for a Ctrl-Break. If none is present, then the program returns from the interrupt to the user code that continues on unabated. (This generates a large amount of overhead, which is why the manual explains that using the **\$U** directive will noticeably slow the user's application.)

Therefore, a section of code is enclosed with a **{\$U+}** at the top and a **{\$U-}** at the bottom, Turbo will insert the INT 3s in front of each Pascal statement. Unfortunately, this is not the preferred INT 1 breakpoint. It is quite easy, however, to patch DEBUG so that the two interrupts operate identically. The procedure for doing this under PC-DOS 3.x is shown in Listing 1, along with a sample program that demonstrates the technique. A similar procedure for performing the same trick on PC-DOS 2.1 DEBUG is shown in Listing 2.

Notice that the INT 1 is required

at the very beginning of the SetSingleStep procedure. Since Turbo has redirected INT 3 for its own uses, it is necessary to point the interrupt back to DEBUG. Fortunately, Turbo does not touch the INT 1 debugger breakpoint. Placing this breakpoint interrupt at the beginning of SetSingleStep gives DEBUG the chance it needs to "correct" INT 3 back to itself.

It should be noted that having the ability to interrupt between every Turbo Pascal statement has uses other than simply single-stepping source code statements under DE-

Rather than allow DEBUG to intercept the interrupt, a profiler points INT 3 to itself.

BUG (as appealing as that might be). One common use for the **\$U** directive is in execution profilers. Rather than allow DEBUG to intercept the interrupt, a profiler points INT 3 to itself. Whenever the program interrupts, the profiler examines and saves the return address. After the program has executed, the profiler can then go back and analyze, usually using histograms, which Pascal statements the program executed and how many times. This can provide the programmer with the information he needs to optimize Turbo Pascal program execution.

Next month I am going to move away from **INLINE** interrupts and begin examining virtual memory techniques under Turbo Pascal. This will also be my first experience with Turbo 4.0, and I hope you are as anxious to hear about it as I am to report on it. §

*Stephen Randy Davis is a senior systems programmer for a defense contractor in Greenville, Texas, where he programs various microprocessors. He is also working on his Master's degree in Physics.*

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# The IBM Micro Channel I/O Bus

## Models 50, 60 & 80

by George Morrow

### *The Bus Signals and Their Relationships*

Largely through the use of its Micro Channel I/O bus, IBM intends to regain the dominance it once enjoyed in the desktop microcomputer market. Integrated circuit manufacturers, systems houses, and

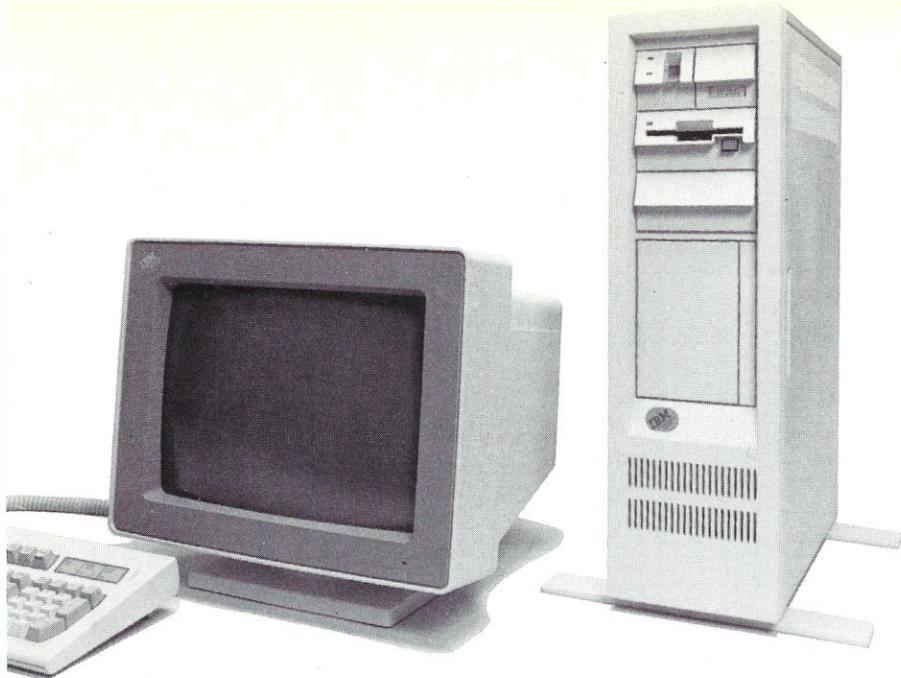
clone makers are all scrambling to unravel the complex web of copyrights, patents, and trade secrets that IBM has spun around its new bus.

Amid all the legal hullabaloo, technical specifications for the bus and the design details needed to build board-level plug-in products have received scant attention. This article is an entry-level tutorial to correct this situation.

It is important to note that I/O buses fall into two broad categories: *synchronous* and *asynchronous*. A synchronous bus uses edges of a special signal, called a *master clock*, which has edges that synchronize changes in data, status, address, and strobe signals. It is also used to delineate the stable periods of these same signals. The Nu-Bus, recently adopted by Apple for its Mac II, is an example of a synchronous I/O bus.

An asynchronous bus has no master clock. The SCSI (Small Computer System's Interface) bus is perhaps the most popular of today's asynchronous buses. And like most asynchronous buses, SCSI uses a set of interlocking, bus *handshake* signals to control data transfer sequences. The Micro Channel, analogous to SCSI, is an asynchronous bus, but it uses no handshake signals of any type. The advantage is that data transfers occur much faster. However, targets and sources of information have no positive feedback to indicate that data actually changes hands. This means the Micro Channel creates an environment that places greater demands on the skills of board-level product designers.





## Organization of Micro Channel Connectors

The Micro Channel accommodates three different connector types (Figure 1), each physically organized into two rows, A and B. The 16-bit connector has 112 pins, and its organization acts as a building block for the other two types. The video connector has a 20-pin extension above the basic 16-bit core. The 32-bit connector extends the 16-bit layout in both directions: a 62-pin address and data extension at the bottom and an 8-pin *matched memory* signal group at the top. Thirty-two-bit connectors are present only on the Model 80.

The Model 50 has one video connector and three 16-bit connectors. The Model 60 has one video connector and seven 16-bit connectors. Finally, the Model 80 has one video connector, four 16-bit connectors, and three 32-bit connectors.

Notice that the 16-bit connector (Figure 1) has three distinct subsections: an 8-bit section with 90 pins and a 16-bit section with 20 pins. Between the two is a 4-pin *key*. This organization suggests that IBM has formulated plans for a low-cost addition to its PS/2 family featuring a modified Micro Channel using an 8-bit-wide data bus.

The Micro Channel connector contacts are spaced on 0.05-inch centers; exactly half the distance between the connector contacts used in the original PC, PC/XT, and PC/AT family. IBM has taken great pains to suppress Electro-Magnetic Interference (EMI) by dedicating a large number of connector pins to ground and power signals. Also, there are generous ground planes on the motherboard between and around the Micro Channel bus connector sites.

The cards are almost 40 percent smaller than those used in the PC/AT, with a usable circuit area of approximately 30 square inches. Since the connectors are more compact and have closer contact spacing, designers of add-on card will have to devote considerable care to the dimension tolerances of the bus contact fingers that make up the card's edge connector. Figure 2 provides

overall dimensions and physical characteristics for the 16-bit, video, and 32-bit memory cards.

Although the Micro Channel's bus logic can accommodate add-in cards of considerable power and versatility, the physical area within which the designer has to work is quite limited. So, if the full power of the Micro Channel is to be realized, standard integrated circuits will be of little use as building blocks in this new environment. Instead, more of a card's logic will have to be placed in silicon, which may encourage vendors of IC-design automation software to hasten their efforts to port standard cell and gate-array integrated circuit design tools onto 80386 PC-type work stations. A happy thought, indeed.

## Micro Channel Bus Logical Organization

Micro Channel bus signals fall into several classes: data, address, status, control, interrupt, bus master, video, utility, power, and reserved pins. Bus master signals provide the mechanism that allow more than one *master* to control events on the bus; a very powerful concept that we will explore later.

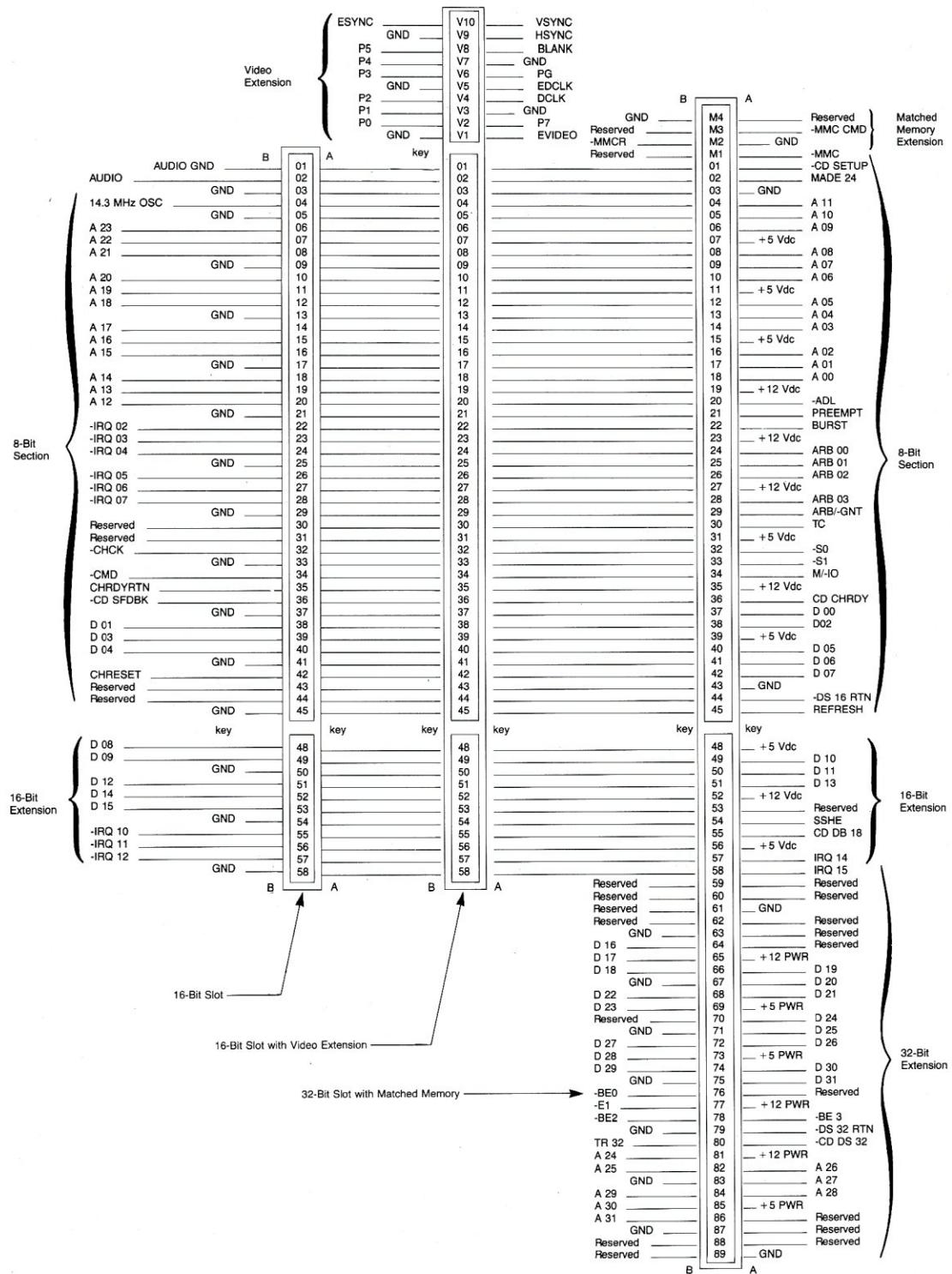
Within these signal classifications are signals I have labeled *non-bus*. Technically, these signals are not part of the Micro Channel since these pins are not *bussed* together between connectors but are wired separately and independently to logic on the motherboard. However, since they are essential to the functional characteristics of the Micro Channel, they form a vital part of its logic. Therefore, *non-bus* signals will be discussed as if they were a part of the Micro Channel.

## Micro Channel Signal Descriptions

The digital voltage levels on the Micro Channel are identical to standard Transistor-Transistor Logic (TTL). A logical zero is any value between 0 and 1 volts. A logical one is any value between 2 and 5 volts.

A minus sign (−) is prefixed to names of *negative logic* signals. This type of *signal* is *active* or *true* when its voltage state is a logical zero and *inactive* or *false* when a logical one.

**Figure 1. Micro Channel Slot Pin Definitions**



The signals are organized by signal classification, and the classifications are divided by connector type:

#### Data: 16-Bit Signals.

**D15-D0 (Data bits 15-0):** These lines<sup>1</sup> are used to transfer the low-order 16 bits of data between devices on the bus (the motherboard is considered a bus device). D15 is the most significant bit (MSB) and D0 is the least significant bit (LSB). Eight-bit data transfers use the lower eight data lines, D7-D0. When a bus master is to receive data, i.e., a bus-read cycle, an addressed slave drives the appropriate data lines, commencing at the leading edge of either -CMD or -MMC CMD (bus command strobes discussed below). The appropriate subset of D15-D0 that participates in the transfer must be stable prior to the trailing edge of -CMD (or -MMC CMD). Furthermore, it must remain stable until the command changes to its inactive state. When a master sends data to a slave, the appropriate data bits must be stable prior to the leading edge of -CMD (or -MMC CMD) and must remain stable until either the master or the slave becomes inactive.

#### Data: 32-Bit Signals

**D31-D16 (Data bits 31-16):** These lines have the same characteristics as D15-D0, above. They are the high-order 16 bits of the Micro Channel's Model 80 32-bit data path and are used, along with the low-order 16 bits, to communicate with 32-bit-wide memory cards.

#### Address: 16-Bit Signals

**A23-A0 (Address bits 23-0):** These lines are driven by the currently active bus master<sup>1</sup> and are used to address both memory and I/O devices attached to the Micro Channel. A23 is the MSB while A0 is the LSB. Neither addresses nor status signals (discussed below) remain valid during an entire bus cycle. Therefore, cards that require some subset of these signals to be stable throughout a given cycle may use either the trailing edge of -ADL (discussed below) or the leading edge of -CMD (or -MMC CMD) to latch the desired status and address signals. I/O devices do not use address bits A16-A23. However, they must fully decode A15-A0.

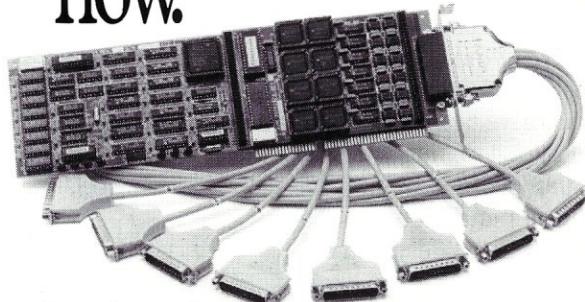
#### Address: 32-Bit Signals

**A31-A24 (Address bits 31-24):** These signals have the same characteristics as A23-A0 above. A31 is the MSB while A24 is the LSB. These signals (along with A23-A0) are used to address memory locations above 16,777,215. A31-A24 contain meaningful data only when the status signal MADE 24 (discussed below) is inactive.

#### Status: 16-Bit Signals

**MADE 24 (24-bit Memory Address Enabled):** This signal<sup>1</sup> is active during bus cycles that access memory locations whose addresses require 24 bits or less to encode. It is false during a bus cycle in which a 32-bit bus master addresses memory greater than 16,777,215.

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**—REFRESH:** This signal<sup>1</sup> is driven from the motherboard. It is active during selected *memory read* bus cycles and is used to refresh dynamic memory attached to the Micro Channel. During refresh cycles, the only address lines with meaningful data are A8–A0. Thus, if the new generation four-megabit DRAMs should be organized with more than 512 rows, they could not be used on Micro Channel memory boards without special logic. The current generation of one-megabit DRAMs must be fully refreshed every four milliseconds. This means that 512 memory refresh bus cycles will occur every four milliseconds. However, there is no guarantee that —REFRESH will occur at evenly spaced intervals. Therefore, the refresh status signal cannot be used for timing purposes.

**M/—IO (Memory/—Input Output):** This signal<sup>1</sup> is driven by the current bus master and is used to distinguish between memory and input-output bus cycles. When M/—IO is high, the current bus cycle is a memory reference. When it is low, an I/O device is being referenced and address bits A32–A16 contain no meaningful data.

**—S1, —S0 (Status bits one and zero):** These two signals<sup>1</sup> are driven by the current bus master. They (along with M/—IO) determine the type of bus cycle in progress (Table 1).

While M/—IO, —S1, and —S0 define eight bus states, only four have been defined. And those that have been defined exactly follow Intel's 8085/8088/8086/80286/80386 signal status protocol. The undefined states reserved by IBM will very likely never be used because bus integrity is enhanced when exactly one of the —S1, —S0 signals is active during a valid bus cycle.

**—CHCK (—Channel Check):** This signal<sup>2</sup> is used to inform the bus that a serious error condition (parity, time-out, etc.) exists. —CHCK can be activated by any device attached to the bus without regard to timing or the current state of the bus. There is provision on the motherboard to use this as a main CPU interrupt.

**—SBHE (—System Byte High Enable):** This bus status signal,<sup>1</sup> along with A0 (Table 2), is used to determine how the high-byte (D15–D8) and

low-byte (D7 – D0) of the bus data will be treated when —DS 16 RTN is active.

## The Micro Channel Non-bus Status Signals and Their Derivations

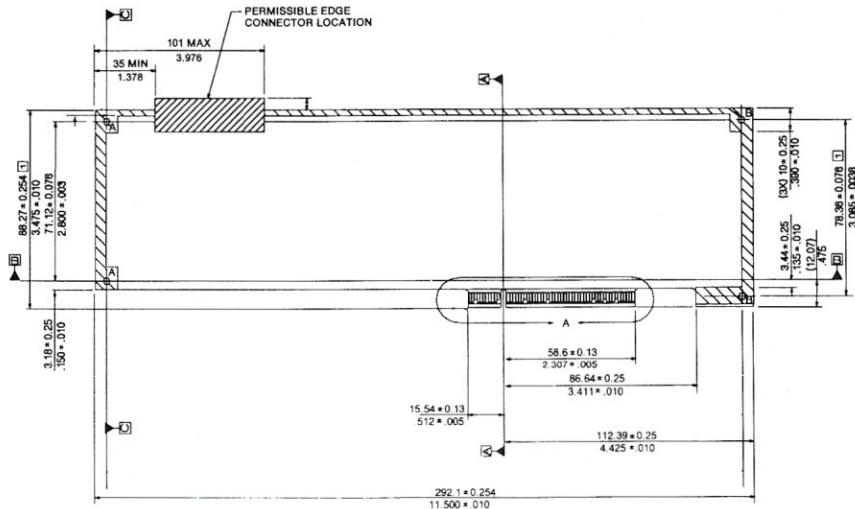
As a general rule, the term *bus* denotes an environment in which the elements (usually connectors) are joined together with a common set of signals, each present at its various elements. The following group of status signals are a subset of the *non-bus* signals that do not follow this rule. They are redundant and closely linked to patents that IBM has licensed from Computer Automation. And from the way they are used, it is clear they are there to exploit these patents, and therefore maximize the legal difficulties for those who might wish to clone the Micro Channel.

Signals with a common name that are unique to individual Micro Channel connectors will carry the suffix (sep) to emphasize that they have a common function but no bus interconnection.

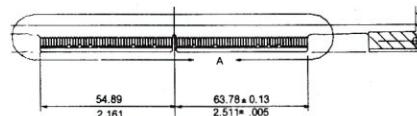
**CD CHRDY(sep) (Channel Ready):** This non-bus set of status signals is generated by cards attached to the Micro Channel that cannot meet the data transfer timing requirements imposed by the bus under all conditions.

**Figure 2. Micro Channel Adapter Dimensions**

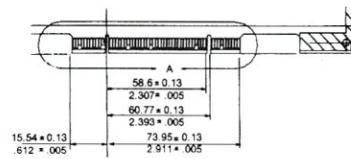
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They are driven by TTL totem-pole devices.<sup>3</sup> Devices attached to the bus that cannot respond to data transfer requests within the specified bus timing must drive these signals false near the start of a bus cycle, just after the address and status signals have stabilized. When enough time has elapsed so that data can be furnished to the bus (or accepted from the bus), these signals are brought to a logical one to inform the motherboard that the bus cycle may be completed.

**CHRDYRTN (Channel Ready ReTurn):** This bus status signal is driven from the motherboard.<sup>4</sup> It is the logical AND of the set of CD CHRDY status signals that emanate from cards plugged into the various connectors. According to IBM, the purpose of this signal is to allow a bus resident master to monitor the overall *ready* status of the bus—all well and good. Why, then, isn't this signal also sufficient for the motherboard? And if it is sufficient, why couldn't the individual CD CHRDY(sep) signals have been done away with? The only answer I can see is that they are a convenient way to get more mileage out of the Computer Automation patents.

**—CD DS 16(sep) (—Card Data Size 16 bits):** These non-bus status signals<sup>3</sup> are generated by motherboard DMA controller *slave cards*, I/O devices or bus-resident memory to inform the motherboard when low, that the currently addressed device's data path is at least 16 bits wide. The set of —CD DS 16 signals is generated by decoding appropriate address and status signals from the bus.

**—DS 16 RTN (—Data Size 16 bits ReTurn):** This bus status signal<sup>4</sup> is generated by the motherboard. It is the logical AND of the set of —CD DS 16 signals emanating from cards plugged into the various connectors. As with CHRDYRTN, this signal allows the current bus master to determine the proper *width* of the data to be transferred in the current bus cycle.

**Table 1. The Status and M/—IO Signals**

M/—IO	—S1	—S0	Bus Cycle Type
1	1	1	not defined (IBM reserved)
1	1	0	memory write
1	0	1	memory read
1	0	0	not defined (IBM reserved)
0	1	1	not defined (IBM reserved)
0	1	0	I/O write
0	0	1	I/O read
0	0	0	not defined (IBM reserved)

**Table 2. System Byte High Enable and A0 States**

—SBHE	A0	Action
1	1	illegal—no data transfer
1	0	transfer low byte (to even address)
0	1	transfer high byte (to odd address)
0	0	transfer both high & low byte (to even address)

**—CD SFDBK(sep) (—CarD Selected FeedBack):** These non-bus status signals are generated by a DMA slave, I/O device, or bus resident memory card attached to the bus to inform the motherboard (when low) that it has been selected. It is a unique and positive acknowledgment to the motherboard that the CarD has been selected as a result of values on the status and address lines. This set of signals is extremely useful in detecting address space conflicts and/or a defective card. —CD SFDBK should be generated by directly decoding appropriate address and status signals.

—CD SFDBK is the first *non-bus* signal that exhibits exceptional functional value. Being able to determine exactly the address region an I/O device or memory card occupies is a perfect tool for diagnostic software to use as a check of system integrity. IBM is to be congratulated for having found such an effective use for this unusual concept. As always, the best ideas are simple ones.

### 32-Bit Status Signals:

**—CD DS 32(sep) (—Card Data Size 32 bits):** These three non-bus status signals<sup>3</sup> are generated by 32-bit memory cards to inform the motherboard, when low, that a 32-bit wide memory device is being addressed. This set of signals is qualified by M/—IO (in a logical true state) and decoded from an appropriate *board select* address pattern.

**—DS 32 RTN (—Data Size 32 bits ReTurn):** This bus-status signal<sup>4</sup> is generated by the motherboard. It is the logical AND of the three —CD DS 32 non-bus status signals discussed above.

**TR 32 (TRanslate 32):** When the current bus master supports a 32-bit data path, this bus-status line is driven false.<sup>1</sup> When TR 32 is true, the main CPU controls the bus and generate —BE3, —BE2, —BE1 and —BE0 (see below). When TR 32 is false, a 32-bit bus master controls the bus. It is responsible for generating —BE3, —BE2, —BE1 and —BE0. TR 32 is driven by the current bus master.

**—BE3 through —BE0 (—Byte Enable Three through —Byte Enable Zero):** During 32-bit memory references, these four bus-status signals<sup>1</sup> indicate which of up to four bytes of data are to be transferred. If —BE3 is low, the high order byte of data, D31–D24, is transferred. If —BE3 is high, the high order data byte is not transferred. Similarly, —BE2 controls data bits D23–D16, —BE1 controls data bits D15–D8, and —BE0 controls data bits D7–D0.

### Matched Memory Signals

Bus cycles that transfer eight or sixteen bits of data require four CPU clock cycles (250 nanoseconds on Model 80s and 333 nanoseconds on Model 60s or 50s). However, the Model 80 supports a special *matched memory* 32-bit memory data transfer that requires only 187 nanoseconds (three CPU clock cycles). The Micro Channel includes a bus status signal and a set of three non-bus status signals to support this three-clock-bus cycle.

**—MMCR(sep) (—Matched Memory Cycle Request):** These are three non-bus status signals,<sup>3</sup> one for each 32-bit connector. A 32-bit wide memory card that can transfer data at a sustained rate of 32 bits every 187 nanoseconds would, when addressed, drive one of these signals false to request a matched memory cycle.

**—MMC (—Matched Memory Cycle):** When the current master (a) supports a 32-bit wide data path, (b) has the capability to execute matched memory bus cycles, and (c) is executing a bus cycle that addresses a 32-bit-wide memory card that has requested a matched memory cycle, the current master drives this bus-status line<sup>1</sup> false.

### Command: 16-Bit Signals

**—ADL (—Address Decode Latch):** This signal<sup>1</sup> is driven by the current bus master. Bus address and status signals are guaranteed to be stable throughout the active period of this signal. If —ADL is buffered through an inverter, such as a 74AS04 or 74ALS04, the resultant signal can be used to enable a D-type transparent latch to buffer and store bus address and status information. Unfortunately, —ADL is not a universal solution to the problem of extending the stable period of address and status information since it is not active during matched memory bus cycles.

**—CMD (—Command):** This is the data transfer command signal for the non-matched memory cycles. When the current master is writing to a bus slave, —CMD delineates the period for which data will be valid on the bus. During a cycle in which a master is seeking to acquire data, the leading edge of this signal commands that the addressed slave place its data on the bus. After so doing, the data must remain stable until the trailing edge of —CMD. As with —ADL, this command line is not active during matched memory bus cycles. —CMD is driven by the current bus master.<sup>1</sup>

**CHRESET (Channel RESET):** The motherboard

generates this bus command signal.<sup>1</sup> It is active when power is applied to the system and during periods of low line voltage. It can also be activated by the main CPU under program control. All devices attached to the Micro Channel use this signal to initialize and reset themselves in preparation for system operation.

### 32-Bit Signals

**—MMC CMD (—Matched Memory Cycle Command):** This is another data transfer bus command signal,<sup>1</sup> generated only during matched memory bus cycles. It functions exactly the same as —CMD and is driven by the current master. —MMC CMD and —CMD are never active during the same bus cycle.

### Interrupt: 16-Bit Signal

**—IRQ 15, 14, 12, 11, 10, 9, 7, 6, 5, 4, 3 (Interrupt ReQuest):** These 11 signals are used by cards attached to the bus to generate interrupt requests. They connect to an interrupt controller on the motherboard that communicates directly with the main CPU. However, if the main CPU is programmed to ignore one or more of these signals, nothing prevents an add-in card from servicing bus-generated interrupt requests. These lines are driven by one or more add-in cards.<sup>2</sup> The priority of these signals, starting at the highest level in descending order, is as follows:

—IRQ9, —IRQ10, —IRQ11, —IRQ12, —IRQ14,  
—IRQ15, —IRQ3, —IRQ4, —IRQ5, —IRQ6, —IRQ7.

Since each signal is generated with open collector logic, more than one device may share the same interrupt-request level.

### Bus Master: 16-Bit Signals

**ARB3-ARBO (ARBItration 3-0):** These four signals represent addresses for up to 16 bus masters (eight

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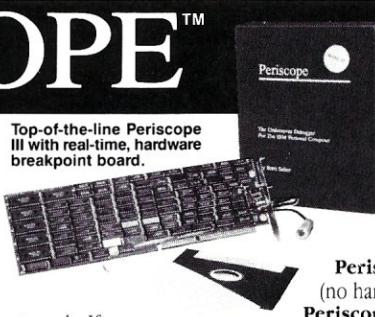
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are reserved for the DMA controller on the motherboard). ARB3 is the MSB and ARB0 is the LSB for these bus master addresses. The highest address, hex F, has the lowest priority and the lowest address, hex 0, has the highest priority.

Each bus master attached to the Micro Channel must drive some subset of these lines.<sup>2</sup> Devices contending for control of the bus are allowed to change the state of these lines for only a short time just after the rising edge of ARB/—GNT (discussed below). If, during this period, a contending master should find that another master has a higher priority on a given ARB line (i.e., the given ARB line is low, but not because of this master), it must refrain from driving all other ARB lines of lower significance. For example, suppose master #1 has an arbitration priority address of hex C (1100 binary) and is contending with master #2 to control the bus, but master #2 has arbitration priority address of hex B (1011 binary). Master #1 has lower priority on ARB2 and therefore must refrain from driving ARB1 and ARB0. The ARB signals are bidirectional: bus masters must be able to monitor these lines as well as drive them.

**ARB/—GNT (ARBitrate/—Grant):** This command signal is high during periods when bus masters are allowed to contend for control of the bus. A bus master “request to contend” for control of the bus is granted at rising edges of ARB/—GNT. It does not actually contend until after this signal has achieved a state of logic one. ARB/—GNT remains in a high state long enough for contending bus masters that are driving the ARB3—ARB0 lines to resolve their priority differences. When these priorities have had time to resolve themselves, ARB/—GNT changes state from high to low. This falling edge is a signal that grants the bus to the contending bus master with the highest priority. During the period that ARB/—GNT is low, the winning bus master continues to drive the ARB3—ARB0 priority address lines. ARB/—GNT is generated by the motherboard.<sup>4</sup>

IBM calls the aggregate logic on the motherboard that creates this signal the “Central Arbitration Control Point” (CACP). This logic does not let ARB/—GNT change from logic zero to one until —CMD, —MMC CMD, S1, S0, and —BURST (discussed below) become inactive. When these conditions have been met, ARB/—GNT changes to logic one (a) if —PREEMPT (discussed below) is active or (b) when —PREEMPT becomes active.

**—PREEMPT:** This bus master arbitration request signal is driven by arbitrating bus masters.<sup>2</sup> All contending bus masters, including the main CPU and the motherboard DMA controller, drive this line low when they wish to arbitrate for control of the bus. A given master stops driving this line upon being granted control over the bus.

**—BURST:** This bus master status signal is used by contending bus masters as a “block transfer” request. A bus master drives this line low upon being granted control over the bus. It remains active until the bus cycle that marks the final data transfer of the block. This signal<sup>2</sup> is driven by bus masters that have the capability to

move blocks of data.

**—TC (Terminal Count):** This motherboard DMA controller bus master signal<sup>4</sup> is active at the end of block transfers when the motherboard’s DMA controller is the current bus master and is moving a block of data to or from a slave DMA device. —TC is pulsed to a logic zero during the final data transfer of a block as a signal to the slave that the terminal count of the data block has been achieved.

## Utility: 16-Bit Signal

**—CD SETUP(sep) (—CarD SETUP):** This non-bus set of utility status signals is generated by all add-in cards.<sup>3</sup> They are used only during system initialization by the main CPU to configure and interrogate a bus device as to type, address range, etc. Just as with —CD SFDBK, —CD SETUP is of great value during initialization because it allows the main CPU to resolve many of the most common type of bus conflicts. This group of signals also allows the operating system to reassign I/O addresses, fill odd holes in memory, and the like.

## Conclusion

This list of Micro Channel signals is not complete: the video signals were left out completely and only a single utility signal was included. Our purpose here, however, is to promote an understanding that will facilitate the design of add-in cards for this new bus. With the signals listed above, most of the tools necessary for this job are at hand. In future articles we will explore ways to use them. §

*George Morrow, the founder and chairman of Morrow Designs that was a leading computer manufacturer for 12 years, is widely known for his knowledge of microcomputer system design. He chaired the IEEE-696 (S-100 bus) standards committee. George is currently chief scientist and a vice president of Nestar Systems where he designs PC and PS/2 high-performance disk and file-server products.*

## NOTES:

<sup>1</sup> Driven with tri-state logic that can source at least 2.6 milliamperes (ma) at no less than 2.4 volts and sink at least 24 ma at no more than 0.4 volts.

<sup>2</sup> Driven with open collector devices capable of sinking at least 24 ma at no more than 0.4 volts.

<sup>3</sup> Driven by TTL totem pole devices. Output must either sink at least 6 ma at no more than 0.4 volts (low-level logical zero) and source at least 400 microamps at no less than 2.4 volts (high-level logical one) and *cannot* be disabled.

<sup>4</sup> Driven by TTL totem pole devices that can source at least 2.6 ma at no less than 2.4 volts and sink at least 24 ma at no more than 0.4 volts.

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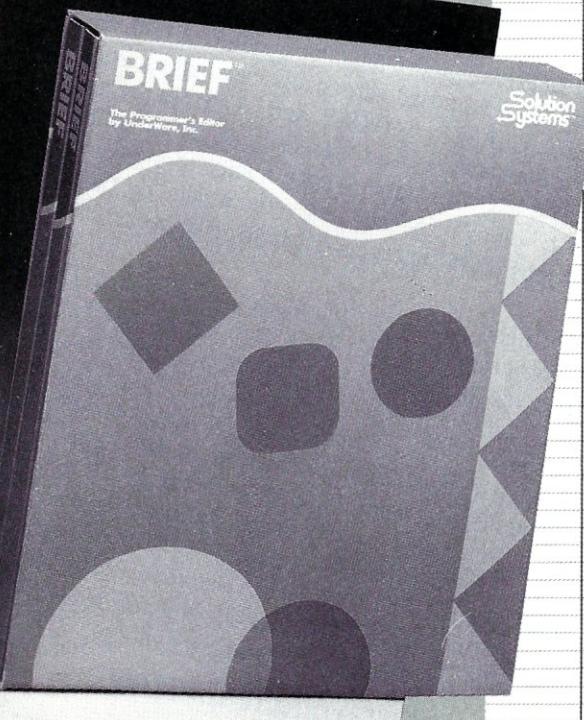
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by Marshall Brain

*By adding capabilities, standard Turbo Pascal routines can be programmed to run in protected mode.*

In the January/February 1987 issue of *M/SJ*, I discussed techniques that can be used to take Turbo Pascal programs in and out of protected mode on an IBM AT. In that article, I explained and demonstrated many of the techniques needed to actually switch the 80286 into its protected mode, so that experimenters could begin to use protected-mode features.

In this article, I will discuss several new capabilities that can be added to the system. These capabilities include: (1) a greatly improved fault handler; (2) the ability to access most standard screen I/O capabilities, such as WRITELN, CLRSCR, GOTOXY, and so on; (3) the ability to access standard keyboard I/O routines, such as READ(KBD) and READLN; and (4) the ability to switch back and forth between real and protected mode "on the fly," so that most DOS functions (such as disk access) can be used.

With these added capabilities, many standard Turbo Pascal programs can be made to run in protected mode, and it is much easier to experiment in protected mode with the addition of the I/O capabilities. This article explains these added capabilities and provides a code listing that demonstrates the steps required to use them.

I would like to point out that, as in the last article, all the code cited here has been tested using Turbo Pascal, Version 3.00B, on an IBM AT using PC-DOS 3.0. Several cautions from the first article are also repeated at the end of this article, as are a list of books and articles you may find helpful when working in protected mode.

## Adding a Better Fault Handler

In the first article, a very primitive fault handler was supplied, which merely beeped and shut down the system. In this article, a more advanced fault handler is pro-

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vided. This is useful because the 80286 has a large number of faults, and because the 80286 provides an error code and address information for most of these faults. This information can be valuable in debugging.

Using the new fault handler, three things happen. First, the screen is cleared. Then, the fault name, such as "Invalid Opcode," is displayed, along with the error code, the segment and offset of the faulting instruction, and the contents of the flags register at the time of the fault (all in Hex). The AT is then returned to DOS (or the Turbo environment) in the real mode. It is useful to have a good book on the 80286 available when attempting to interpret the error codes produced by this chip.

To implement the fault handler, all 14 faults in the IDT must be routed to 14 separate fault handling routines. This allows the specific fault number to be detected. These 14 fault handlers then call a standard FAULT routine that displays the error and returns to the real mode.

## Adding Screen I/O Capabilities

Making screen I/O statements, such as CLRSCR, GOTO-XY, and WRITE, available to Turbo programs running in protected mode is fairly easy since Turbo accesses all of its screen I/O functions through the AT BIOS rather than through DOS. Because the AT BIOS is written to run in protected mode, the code can be made available to the Turbo program by simply modifying the GDT and the IDT.

In order for BIOS code to be accessed by Turbo, the address of the BIOS video routine must first be stored

while in real mode. This is done near the bottom of the code listing in the routine GET\_INT\_ROUTINE\_ADDRS. This routine accesses and stores all of the BIOS and hardware interrupt code addresses from the real mode's interrupt vector table because they will be needed by the IDT and GDT. The BIOS video I/O routines are accessed at the address stored in vector 10h of the real mode interrupt address table.

Once this address is stored, it is used to create an IDT interrupt gate. This gate is a descriptor in the IDT that points indirectly to the video routines. In the routine SETUP\_IDT, vector 10h is set to point to the video code. When an interrupt 10h occurs, two things happen. First, the IDT entry for 10h is accessed to see what code should be executed for this interrupt. The IDT entry gives a code offset to jump to, as well as a code segment. In this case the segment is called VIDEO\_DESC. This segment value is loaded into the CS register, which then causes step two to occur—a segment descriptor is loaded from the GDT. VIDEO\_DESC is a constant set to 88, which is descriptor number 11 in the GDT. This descriptor in the GDT contains the segment descriptor used to actually access the code in the BIOS (ROM) area.

This arrangement allows the correct code to be accessed whenever a video interrupt takes place in a Turbo program that is running in protected mode. However, two data areas must also be made available. The first is the BIOS data area starting at address 400h. The second is the screen memory buffer area for either the monochrome or graphics display adapter. Both of these memory areas are made available by creating descriptors in the GDT at the specific addresses expected by code that is normally running in real mode. For example, real mode code that tries to access memory at address 400h normally does so by loading a 40h into a segment register. This works well for protected mode programs as long as descriptor 8 (40h) is reserved and made to point to memory at 400h. The same logic holds true for the display memory buffers.

Once these additions are made to the code, access to BIOS screen I/O routines takes place in protected mode in the same way it does for real-mode programs. There are some slight problems with the EGA card, however, because the IBM EGA replaces the normal video BIOS routines with the EGA's routines.

## Adding Keyboard I/O Capabilities

Adding the keyboard I/O capabilities found in real-mode programs is very useful to protected-mode programmers, and it is only slightly more difficult to do than it is to add in the screen I/O routines.

First, IDT gates must be created to allow access to the keyboard BIOS routines. This is done using the techniques described above. The keyboard routines also use the BIOS data area, but since this area has already been made available for the screen I/O routines, nothing further needs to be done.

The keyboard I/O capability does require one step not

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needed for the screen I/O capability; the keyboard I/O capability requires that a hardware interrupt generated by the keyboard be recognized. This hardware interrupt normally comes in on interrupt vector 9 in real mode.

To make the keyboard hardware interrupt work in protected mode, the interrupt mask must first be changed so the keyboard interrupt is allowed. The AT BIOS routine that switches the AT to protected mode automatically masks all interrupts so the AT cannot be disturbed while in protected mode. The keyboard interrupt can be reenabled by setting bit 1 of interrupt controller 1's mask byte to 0. This is accomplished by a single line of code in the GOTO\_PROTECTED procedure.

Once this has been done, the interrupt can be recognized by the AT. The code to handle that interrupt is made available by creating another gate in the IDT. You can see this occurring in the SETUP\_IDT routine for vector 61h. (Remember that the hardware interrupt vectors from the two hardware interrupt controllers can be mapped anywhere in the vector space; two parameters in the GOTO\_PROTECTED procedure remap these vectors to 60h and 70h. This was discussed in the January/February 1987 issue of *M/S*.)

With these changes in place, all keyboard I/O functions in Turbo Pascal are available. You may also notice that the same techniques have been used to enable the Timer Tick hardware interrupt in protected mode. These techniques also could be used to enable other hardware interrupts.

## Switching Back and Forth

One of the nicer features of the AT is that the BIOS code seems to have been written with the protected mode in mind. Most of it runs without problems when Turbo Pascal switches to the protected mode. Unfortunately, the same is not true for DOS, which uses hundreds of different values in the real-mode segment registers.

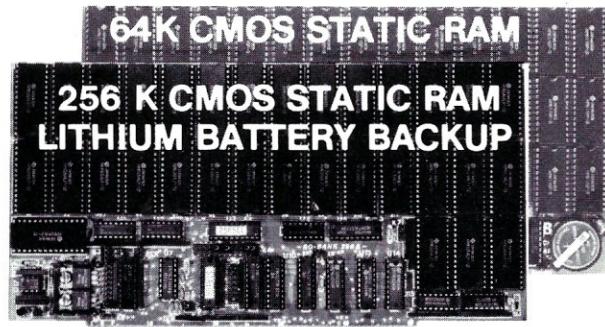
Because DOS is so unruly, it would be almost impossible to modify it to run in protected mode; therefore, Turbo Pascal's disk access capabilities are not available in protected mode. While this can be a problem in some cases, it is often possible to avoid the issue by simply switching the AT into real mode long enough to allow the required disk accesses to take place. The AT can then be switched back into protected mode.

This is now possible using the routines GOTO\_REAL and GOTO\_PROTECTED. To initially go into protected mode, call GOTO\_PROTECTED. To switch to real mode, call GOTO\_REAL and do whatever needs doing. Then switch back to protected mode with the same GOTO\_PROTECTED. Since it is important to always be in real mode when the program is exited, the error handler does this automatically.

## Conclusion

Listing 1 demonstrates in the DO\_TESTS routine several of the capabilities mentioned in this article. Several cautions should be mentioned for those who use this code. First, typed constants, which reside in the code

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segment, cannot be written to while Turbo Pascal is in protected mode because protected mode does not allow modification of the code segment. Also, you should try to have no memory-resident software loaded when you are experimenting in protected mode. Finally, leave the compiler directives set the way they are in the listing.

The only major Turbo Pascal capability not yet implemented is Heap access. This occurs because the Heap is accessed with a very large number of segment register values in Turbo Pascal. Heap access will be discussed in the next article. §

## References

Brain, Marshall, "Experimenting with Protected Mode on the AT." *Micro/Systems Journal*, January/February 1987.

Claff, William J., "Moving From the 8088 to the

**Listing 1. A demonstration of a Turbo program running in protected mode using normal I/O routines.**

```

program protected mode is demo;
{SU,-k} {These directives MUST be set off like this}

const
  gdt_size=$1700; {Max number of descriptors in GDT minus 1}
  idt_size=$75; {Max number of descriptors in IDT minus 1}
  code_desc=$148; {Code segment descriptor #4 in GDT}
  bios_desc=$156; {Bios code segment descriptor #5. It is
  created by int 15h, function 89h}
  video_desc=$188; {Video desc is created to handle ega BIOS if works}
  const {The following constants are variables stored in the segment}
  data_seg:integer; {Storage space for segment registers}
  stack_seg:integer = 0;
  extra_seg:integer = 0;
type
  string80:string[80];
  string5:string[5];
  descriptor:tDescriptor; {from AT Bios listing}
  descriptor^:integer; {segment limit (-65536 bytes)}
  base_lo:word;integer; {28 bit physical address (0-[GM-1])}
  base_hi:byte;byte;
  data_act_rights:byte;
  data_reserved:byte; {reserved for 80386 compatibility}
end;
var
  result:record ax,bx,cx,dx,bp,si,di,ds,es,flags:integer; end;
  gdtarray[0..gdt_size]:tDescriptor; {Global descriptor table}
  idtarray[0..idt_size]:tDescriptor; {Interrupt descriptor table}
  mask1 8259;mask2 8259h; {Storage space for 8259 masks}
  {The following are the code offset storage locations into the BIOS
  code offset ($00000000) and data offset ($00000000) used by this program
  while in protected mode. Used mostly in IDT.}
  video_seg:videoofs;time_ofs:timerint;ofs:integer;
  cassette_ticks:keyboardofs;kbd_int_ofs:integer;
  {Storage space for 8259 location}
  ega_ofs:ega_sequinteger;
  {arTays are on top of the screen's memory buffer. Sb800 is
  used for CCA, EGA, and Sb000 for mono. Used by DISPLAY}
  screen:array[0..$2000] of byte absolute $b000:0;
  mono_display:boolean;
  {Variables needed by error handling routine.}
  err,cs,ip,fl:integer; faultnum:byte; errorflag:boolean;
procedure screen_check;
{checks whether Screen is mono or something else for DISPLAY rtn.}
begin
  result.ax:=$0F00;
  intr[$10].result:=7;
  if [result.ax]=7 then
    mono_display:=true
  else
    mono_display:=false;
end;
procedure display(col,row:byte;ln:string80);
{Writes characters in LN onto the screen at the row and column
  indicated. The characters are written directly into memory.}
var x,addr:integer;
begin
  addr:=row*80+col;
  for x:=0 to length(ln)-1 do
  begin
    if mono_display then
      screen[(x+addr)*2]:=ord(ln[x+1])
    else
      screen[(x+addr)*2]:=ord(ln[x+1]);
  end;
end;
function hex(val:integer):string5;
{Converts VAL into a hexdecimal string.}
var ln,num:string[16]rbyte;
begin
  num:='0123456789ABCDEF';
  x:=hi[val] shr 4; ln:=ln+num[x+1];
  x:=hi[val] and $0f; ln:=ln+num[x+1];
  x:=lo[val] shr 4; ln:=ln+num[x+1];
  x:=lo[val] and $0f; ln:=ln+num[x+1];
  hex:=ln;
end;
procedure setup_error;
{Displays a message if you try to setup a descriptor outside the
  boundaries of a descriptor table.}
begin
  writeln;writeln('There has been an error during setup of ',
  'descriptor tables.');
  halt;
end;
procedure set_gdt_desc(num,seg_lim,base_lo:integer);
{This procedure sets up descriptor Number NUM in the GDT with the
  values that are passed.}
begin
  if (num>0) and (num<=gdt_size) then
  begin
    with gdt[num] do
    begin
      base_lo:=base_lo;
      base_hi:=base_hi;
      data_act_rights:=data_act_rights;
      data_reserved:=0;
    end;
  end else setup_error;
end;
procedure set_idt_desc(num,seg_lim,base_lo:integer);
{This procedure sets up descriptor Number NUM in the IDT with the
  values that are passed.}
begin
  if (num>0) and (num<=idt_size) then
  begin
    with idt[num] do
    begin
      seg_limit:=seg_lim;
      base_lo:=base_lo;
      base_hi:=base_hi;
      data_act_rights:=data_act_rights;
      data_reserved:=0;
    end;
  end else setup_error;
end;
procedure beep;
{Beeps the speaker.}
begin
  sound(400):delay(200):nosound;
end;
function spaces(x:byte):string80;
var ln:instring80; Y:byte;
begin
  ln:=''; for y:=1 to x do ln:=ln+' ';
  spaces:=ln;
end;
procedure clrscr2;
{Clears the screen manually to avoid a bios call.}
var x:byte;
begin
  for x:=0 to 24 do display(0,x,spaces(80));
end;
procedure show_err_loc(col,row:byte);
{Shows the name of the fault, along with the error code, CS
  IP, and flags pushed on the stack.}
var ln:string80;
begin
  case faultnum of
    0:ln:='Divide error';
    1:ln:='Single step';
    2:ln:='NMI interrupt';
    3:ln:='Breakpoint found';
    4:ln:='Overflow error';
    5:ln:='BOUND Range excep';
    6:ln:='Invalid Opcode';
    7:ln:='No Processor extension';
    8:ln:='Stack underflow';
    9:ln:='Proc ext seg overrun';
    10:ln:='Invalid TSS';
    11:ln:='Segment not present';
    12:ln:='Stack overflow or missing';
    13:ln:='General Protection error';
  end;
  clrscr2;beep;
  display(col,row+1,ln);
  ln:=ERR+hex(err)+' IP='+hex(ip)+' CS='+hex(cs)+' FLAGS='+hex(fl);
  display(col,row+1,ln);
end;
procedure goto_real;
{Returns to real mode by requesting reset signal from 8042. Software
  will eventually end up at protected mode_exitpoint in Real mode.}
begin
  inline($fa); {cl1}
  port[$d4]:=$fe; {create hdwr reset}
  inline($d4); {hlt}
end;
procedure fault;
{This routine is entered if a processor fault occurs while in
  protected mode.}
begin
  inline($58/$58/$58); {pop ax 3 times to elim last call}
  inline($58/$58/$58); {pop ax; move err,ax}
  inline($58/$58/$58);
  inline($58/$58/$58);
  inline($58/$58/$58);
  show_err_loc(1,1);
  errorflag:=true;
  goto_real;
end;

```

... continued on page 56.

FEBRUARY 1988

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# DESQview—Multitasking the Easy Way

by Charles H. Strom

I love to tinker with multiuser/multitasking alternatives to MS-DOS. However, DESQview from Quarterdeck Office Systems has taken the challenge out of such tinkering. As a frequent user of MS-DOS software and a frequent software reviewer, one could say that I am jaded. Rarely does a product come along that truly excites me, but I am delighted to say that DESQview does. I have been an avid DESQview user for years, and Quarterdeck's latest version, 2.00, is nothing short of super.

## What is DESQview?

Unlike Digital Research's Concurrent DOS or The Software Link's PC-MOS (reviewed in *M/SJ*, November/December 1987) DESQview (DV) runs under MS-DOS. DV offers a windowing environment that permits up to approximately 60 programs to be run simultaneously (although why anyone would want to use 60 programs at the same time escapes me) and these, in turn, can open up as many as 255 windows. Needless to say, such processing overhead requires a lot of memory.

DV handles memory in several ways, depending on the CPU under which it is running. Quarterdeck's DV manual includes an excellent tutorial on memory usage that would make an impressive treatise on its

own. I will summarize this discussion as briefly as possible.

A basic DOS system can address up to 640K of memory. Taking DOS and DV memory demands into account, about 435K of free memory is available for all tasks. If the user opens more windows, other processes are suspended and spooled to the hard disk. In addition, 8086/88 and 80286 systems can address up to 15 Mbytes of EEMS (Enhanced Expanded Memory Specification) memory. Expanded memory, also known as Lotus/Intel Specification or LIMS, is a popular method of addressing extra RAM in 16K chunks using a bank-switching technique. Several OEMs have improved on this technique by adding functionality, including the capability to address 64K memory chunks, resulting in the EEMS, or AST/Quadram/Ashton-Tate, specification. DV takes advantage of EEMS memory and allows a substantial increase in the amount of RAM available for running multiple tasks in real time. In addition, part of the DV code itself can be relocated to EEMS memory, increasing the maximum size of any task. Both AST and Quadram offer EEMS boards for both PC/XT- and AT-type machines. Lastly, 80386 systems can take advantage of extended (normal, linearly addressed) memory above the 1-Mbyte address space to emulate

EEMS RAM. Quarterdeck offers a device driver, QEEMS.SYS, to do just this. Actually, QEEMS.SYS emulates EMS memory and adds enough EEMS features to support DV, although it is not a full EEMS emulation. In any event, the combination of an 80386 system with QEEMS.SYS and DV is an impressive combination offering both multitasking and rapid speed.

## Installation

The process of initializing DV is quick and painless. The INSTALL program takes care of transferring the necessary files, setting up batch files, and other functions. An interesting feature allows you to search for applications residing on the hard drive and automatically install those it identifies into the main DV menu. (DV can be used with a floppy-only system, but I did not use it on such a configuration.) After the actual installation, Setup is automatically invoked to select the video adapter type and appropriate mouse information. A mouse is handy but, unlike a lot of other software I have used, there is little penalty for using the keyboard instead of a mouse. An advanced Setup menu can specify parameters for DV's auto dialer, color options, window positions, etc. There is also a performance option that varies time slicing, i.e., the rela-

tive amount of time spent on foreground and background processes. This is particularly useful for such things as tuning communications programs running in the background. In summary, installation takes but a few minutes and requires no technical expertise whatsoever. DV's manual also goes into all options in scrupulous detail.

## Running Under DESQview

DV.BAT brings up the opening screen. It is simple and uncluttered, and allows you to open or close one or more applications, zoom the display of a window to full size, exit DV, get on-line help, and perform other functions. Either the mouse or a keyboard press can be used in all cases. At any time, pressing the Alt key, (user-configurable), will bring back the DESQview control menu. It is a lot more complicated to describe all of this than it is to use DV since the user interface is so intuitive. Additional functions allow you to add or remove applications from the menu; the Mark and Transfer commands (a cut-and-paste method of transferring information from one program to another) and the Change command allow tailoring of applications to maximize their efficiency under DV.

I will describe a few special DV features in no particular order to give a flavor of the impressive flexibility built into the system. DOS services, for example, provide access to many DOS commands and allow operation of the selected tasks in the background. Type, Dir, Print, Append, Format, and other commands are all available from the menu. There is also a simple way to go directly to the familiar C> prompt, while specifying the size of the DOS work area. The Mark function allows any displayed telephone number to be automatically dialed by a Hayes-compatible modem. A Learn feature allows DV to record a series of key-strokes and later play them back by entering a single key-stroke. This is useful both when at the DV command screen level and within any application running under DV.

DESQview is notable in that it will

run virtually any DOS program. Examples range from WordStar, SuperCalc, and dBASE to programs that often cause problems running under environments that are not pure DOS, such as communications programs (I use both Qmodem and Pro-YAM without problems), Microsoft Word (a known troublemaker because it bypasses the operating system), and even Ventura Publisher (a memory hog if there ever was one). The most popular applications are represented by DVP, or DESQview Program Information files. These files are easily accessible for study or modification using the DV Change a Program command. If you wish to run a program not represented by a DVP file, it can be installed by answering a series of questions. This may or may not be a simple task depending on the demands the application makes on the computer's resources. Lastly, Topview PIF files can be used to glean the needed information to enter them into a DVP file. Correct entry of information into a DVP file allows proper allocation of RAM size, concurrent background processing (if desired), running in a small window, and so on. DV also comes with special loader files that permit many popular, badly behaved applications (such as the aforementioned Microsoft Word) to execute properly under DV.

## Support

I don't have a great deal to say on the subject of support for a very good reason; DV is so easy to install and use that I have never needed to resort to outside assistance. There is, however, a customer support plan consisting of several options. When a purchaser registers his copy of DV, he will receive periodic notifications by mail telling him of new versions, additional loaders, and auxiliary products, such as the DESQview Companion series of communications, word processor, and appointment programs. In addition, there is a single-user bulletin board system available free of charge that offers patches, hints, and tips. Quarterdeck also runs a DESQview bulletin board

on Compuserve.

Lastly, a priority service plan is available for an annual fee of \$30 that offers telephone support, discounts on future purchases, extended access to the bulletin board, and other benefits. I did not have an opportunity to try out the priority service plan, but the price is certainly attractive.

## Why Bother?

More than a few people ask me why I bother with multitasking. I usually respond that if you need to ask, don't bother. As simple as DESQview is to integrate into your everyday operation, I cannot say that it is perfect. It is, however, certainly the simplest and most cost-effective way to go if you want to enjoy the advantages of being able to use fancy print formatters without tying up the machine for hours, to download files from GENIE in the background while working on an article in the foreground, etc. DESQview doesn't offer some of the bells and whistles of Digital Research's Concurrent DOS or The Software Link's PC-MOS operating system, nor does it support multiuser operation (although it is possible to run DV on networked machines), but it does have the advantage of ease of use from the perspective of the operator and better DOS compatibility. I strongly recommend it over other products, such as DoubleDOS, because of its simplicity of operation and added functionality. §

*Charles Strom, a chemist by training, has been working with computers for more than ten years. He is a sysop on the GENIE national time-sharing service.*

## Product Information

DESQview Version 2.0 is available through retailers for \$129.95. For more information, contact:

**Quarterdeck Office Systems**  
150 Pico Blvd.  
Santa Monica, CA 90405  
(213) 392-9851

# Quadram's Quadstar LAN

by George Miller

Local Area Networks (LANs) have been expensive and difficult to install and use by those who encounter the technology for the first time. Inexpensive LANs are available, but they tend to be low in performance and features as well as cost. More powerful LANs are often easier to use but they also are harder to maintain.

Quadram now brings its solution to the problem of cost and confusion for first-time LAN customers, QuadStar. QuadStar is based on StarLAN-compatible network cards and the Tapestry network operating system. StarLAN operates at 1 megabyte per second (MB/sec.), 10 times slower than Ethernet which requires coax cable. Tapestry provides an icon-based, customizable user interface. In addition, Quadram has packaged the two in a kit for the first-time user—a complete two-user, two-node network. All parts are included in one box—no fuss, no mess.

QuadStar is an easy-to-install, easy-to-use network with average performance. The initial configuration is capable of supporting up to six computers by just adding network cards. More users can be supported with additional cards and hardware. The network software is set up for up to 12 users. An upgrade also is available for more users.

Quadram has put to-

gether the kind of system that is appropriate for an office that has never before had a network and has a need to share data and peripherals. QuadStar is a one-stop shop where the only decisions to make are how many cards to buy and where to run the wire between the computers.

## Product Overview

The QuadStar package has three parts: Quadram's StarLAN network cards, Tapestry from Torus, and Quadram's installation support. StarLAN is a bus network that runs at 1 megabit per second (Mbps), and uses two twisted-pair wires to connect each station to a common hub. Hubs have a fixed number of connections and the hubs can be linked together. The maximum distance limits and number of nodes depend on the types

of cards and hubs involved. Most telephone wiring can be used to connect a computer to a hub. The QuadStar Starter kit actually comes with a combination hub and network interface on a single card.

The QuadStar kit comes with both a QS-100 and a QS-PH6 network card. The QS-100 is a half-card with one RJ-45 jack. The QS-PH6 is a full-length card that incorporates a QS-100 and a 6 port, passive, StarLAN hub. It has five RJ-45 jacks to connect to five other QS-100 or QS-188 cards. The QS-188 card is a full-length card with a StarLAN interface that includes an 80188 processor with dual-port memory. The 80188 handles the network traffic, thereby providing higher throughput and minimizing host processor overhead due to network traffic.



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Online tutorial	Yes	No	Yes
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Function Key assignments labeled on screen	Yes	No	No
WP Functions	Extensive	Limited	Limited
Complete DOS shell	Yes	No	No
Pop-up Programmer's Calculator and ASCII table	Yes	No	No ASCII
Unlimited 'Off the Cuff' keystroke macros	Yes	No	Yes
Allocates all available memory to compiler when run from within editor	Yes	No	Yes
Intelligent indenting, template editing and brace/parenthesis/block matching and checking for all major languages	Yes	C Only	Limited
Flexible condensed mode display	Yes	No	Yes
Optional background communications and Spell Checker modules	Yes	No	No
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Yes	Yes	No	Yes
Yes	Yes	No	No
Yes	Yes	Yes	No
Yes	Yes	No	No
Yes	Yes	No	No
Extensive	Limited	Limited	Limited
Yes	No	No	No
Yes	No	No	No ASCII
Yes	No	No	Yes
Yes	No	Yes	Yes
Yes	C Only	No	Limited
Yes	No	Yes	No
Yes	No	No	No
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The QS-188 costs more but is appropriate for a server or someone demanding extensive network use. Two QS-PH6 cards can be connected together to provide a 12-computer network. Large networks require an active, external hub with 12 connections which Quadram also sells. More than two active hubs can be connected together for large networks. There is a distance limitation using QS-PH6 cards; all nodes must be within 800 cable feet of each other. Therefore, one node could be 600 feet from the hub while all others must be 200 feet or less. Keeping everyone within 400 feet makes things easy.

Tapestry is a network operating system that works with a variety of network interface cards, including Ethernet and Arcnet. Tapestry provides distributed services on non-dedicated servers. It requires a single master server, but any type of service can be placed on any computer in the network. A printer can

be attached to one machine while a modem is attached to another. These can be shared from any computer on the network. The advantage of this approach is that services can be placed within a network where they are most convenient, such as having the computer positioned next to the printer be the print server. The disadvantage is that a service is only available when the computer is on and running Tapestry—Ctrl-Alt-Del on a server may cause screams from down the hall.

Tapestry installs itself between DOS and applications. It watches application requests to DOS to see if any are destined for the network and processes them accordingly. Tapestry is also an icon-based, front end to DOS. There is even a simple text editor supplied with Tapestry. Other application programs can be installed and run from the application menu. An application is run by selecting the appropriate icon. The application can be set up to run only on certain types

of computer configurations like color-only applications. Tapestry detects the type of computer and prevents applications from running on improperly configured machines. It is also possible to use the DOS COMMAND program for those more comfortable with A>.

This approach to networking means that a user need never know about DOS, since applications can be started directly from a menu. All network configuration options are available through the main menu, which makes Tapestry appear to be an integrated software package. Although a mouse is optional, it can make some tasks easier than using the keyboard.

Tapestry can provide multiple file servers. Drive H: is reserved for read-only Tapestry files. Drives I:, J:, K:, and L: are assignable network drives. Network file services are provided in terms of cabinets and drawers. Drawers are named and have limited-access protection levels, plus password protection. A network drive can be set to any drawer. A drawer looks like a normal DOS disk to applications. Installed application programs are placed on H:. Cabinets are placed on a server's local disk. However, it is not possible to make existing subdirectories into drawers. Files must be moved into a newly created drawer and deleted from the source directory. A backup and restore option using floppy disks is available.

Print servers also are available with print spooling capabilities normally found in a network. However, Tapestry only supports LPT1: as a network printer. Other printers are local only. The designated print service for a computer can be changed at any time. Tapestry supports printer initialization along with printer descriptions, such as MATRIX or LASER. Location information can also be specified, such as FRONT OFFICE PRINTER.

A mail system is provided along with a text editor that can be used for general editing. The editor will not displace Microsoft WORD or Word Perfect, but it may be ade-

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quate for many people. The mail "in" and "out" basket icons change, depending upon their contents, so it is apparent when mail is received. Status messages can be displayed in the upper left portion of the screen when mail is received. A short, one-line message can be sent in the same fashion, but it is only displayed and not logged into the mail system. This is useful for status messages such as TIME FOR LUNCH. Mailing lists and message retention limits also are available.

Tapestry even comes with a communication gateway option. This allows access to Telex and electronic mail services, such as MCI. It can also be used to call bulletin boards or other PCs. The connections can be made directly between computers or through modems. Autodial modems are supported, and customization for non-Hayes modems is provided. Only one modem is allowed per communication gateway. The modems are shared on a first-come-first-served basis and a directory entry in a user's address book specifies which communication service to use. This allows specific connections to be made using a particular modem. Multiple communication services can be configured using multiple PCs. A communication server can also have file and printer support, too.

The communication service uses a terminal emulation program. It is a simple program with XMODEM file transfer capability, text file capture and transmission, and a limited macro facility, including an auto-login capability. Creating and editing macros is tedious but workable.

Tapestry has a variety of other, less important options available through icons or function keys. The interface is intuitive, but often confusing when you cannot move to a field or icon you think should be available. Help is context-sensitive and is available via F1. Tapestry is a very complete package. All the pieces are fully functional, but limited. Tapestry is capable of handling two to 20 users with little alteration. Larger groups can be handled if the network load is light, but more capa-

ble network systems may be more appropriate for larger groups.

## Documentation and Installation

Quadram's main contribution to the product is its packaging and installation procedure. It effectively makes network installation simple, which is not an easy task. The Starter Kit comes in one box with separate boxes that contain the QS-100 and QS-PH6 cards. Two Tapestry manuals are included; one for the network manager and the other for a user. A number of other small booklets and pamphlets are included, plus

### *Tapestry installs itself between DOS and applications and watches DOS requests.*

a single audio cassette.

My recommendation is read the directions first, even if you have installed Tapestry or StarLAN before. Quadram has set up the installation procedure so that the QS-100 card must be placed in the computer as the initial network server, and the QS-PH6 goes in the other workstation. It does not work the other way around. I installed a QS-188 after the Starter Kit was installed.

If you are confident, you can use the pamphlet with 10 simple steps on it. All that is necessary is the Starter Kit, a screwdriver to open the computers, an empty slot in each computer for the network cards, and a hard disk on the server with at least 4 MB free. The computers should be within 20 feet of each other since the cable provided in the kit is only 25 feet long. Longer ca-

bles are available from Quadram. Just follow the directions and you should be up and running within two hours, one if you are quick. Additional workstations can be added in under half an hour, not including cabling time, which varies depending upon whether the cable just runs along the floor or goes through walls. One warning, check out network card addresses if you have EMS RAM cards. The default configuration for both memory buffer addresses tend to use D000 hex.

For those who like to take a little more time or just want to be sure, there are manuals on how to get started and the cassette tape. The tape is designed to be played while you are putting the system together so a portable tape player is needed. The tape even tells you when to pause so you can concentrate on working with the hardware and software. Like the pamphlet, the tape starts from opening the box and finishes with a completely installed, running, two-node network.

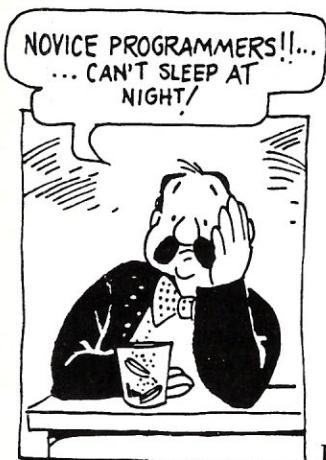
The installation documentation is complete, and most common problems and their corrections are well presented. However, more difficult problems such as bad cable connections or defective boards, will normally take a call to Quadram's support service, which is available during the normal work week.

The Tapestry documentation is generally well presented and organized. Finding something using the index is easy, if you have the right terminology. There are some cross-references, but some of the Tapestry network jargon can cause some page flipping. The descriptions of the services, however, are complete and understandable.

Quadram's documentation comes with plastic ring binders that are best left in the box because you will probably use them once and put them away. The Tapestry manuals, on the other hand, are the more conventional IBM PC-style documents with binders and covers.

Short 25- and 50-foot cables are provided with each network adapter card. This is sufficient for open of-

# Got Software Problems?



	Full Version	Starter Version	Cost of Upgrade for \$99 version
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<b>Context-Sensitive Help</b>	Yes		50
<b>Command Window</b>	Yes		50
<b>Relational Model</b>	Yes		150
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fices or computers within the same area. Longer cables are available from Quadram, but special cables may need to be made for distances of more than 100 feet. Using telephone wire within the walls is possible with certain limitations. Twisted pair telephone wire is preferred. However, this type of wire is not always used. In any case, almost any telephone wires can be used for short distances. Remember that you will need four wires for StarLAN.

## Network Operation

Running a QuadStar network is relatively painless once the system is installed. The normal mode of operation is to bring up the main server and then all the other servers. Users are then free to log in and log out as necessary. Network services can be disabled and a server should not be turned off unless all services are disabled and not in use.

## Performance

Performance of network services depends greatly on overall network use. The 1 MB/sec. StarLAN is faster than a floppy disk transfer rate but five times slower than a hard disk. However, the latter does not take into account the latency of a hard disk, only its transfer rate. The performance of the file server can be enhanced by a faster computer, a fast hard disk, and disk-caching software with a large buffer. The performance may not be as fast as a high-performance, local hard disk, but the network can come close.

QuadStar and Tapestry perform well with a small load. The system should handle six users with no trouble. More users will require more detailed network planning and may require multiple file servers, local hard disks, or local RAM disks. File services should be more than adequate if the file servers are used intermittently.

The mail service seems to provide little load to the network and QuadStar can easily handle dozens of users. The same holds true for the print services. Print operations may actually free up computers faster because

of spooling to the print server's disk.

The only service that has a noticeable delay is the communication service. This is to be expected of just about any network system because most communication services are full duplex, which means a typed character goes across the network to the remote computer, back to the communication server, across the network again, and onto the screen. Listing data from the remote source displays smoothly because the data moves in one direction only. In general, the communication service is usable, even with a heavily loaded

*QuadStar and  
Tapestry  
should handle  
six users. More  
users will  
require more  
planning.*

network, but the gateway server should be dedicated as a server, otherwise echo speed and throughput will suffer.

## Security and Maintenance

Network security is implemented using passwords for log in and access to individual services. Services can be locked from the server on which they reside as well as certain controls available only on the network master server.

Services and network disks can be saved and restored using utilities supplied with Tapestry. Backup and restore can be selective, but they only work with floppy disks. Tape backup software must be compatible with the network disk systems. Tape backup software, which goes directly to the hardware or BIOS, may not work properly with network disks.

Utilities are provided to com-

pletely remove Tapestry and its services from a computer. Transferring services across the network to another computer is not supported directly.

## Summary

If your company or one of its customers desperately needs a network but is daunted by the expense, the QuadStar Starter Kit at \$1,095 offers an inexpensive initiation into the world of LANs. Of course, you will want to look at Novell, 3Com, or Banyan VINES if the performance needs or number of users is high. The key feature of QuadStar is that it is so easy to install.

Although the Starter Kit uses a QS-100 for the network server, I would recommend getting a QS-188 for the main file server. Also, if you plan on using an 80386 machine on the network, get a QS-188 for it too since the QS-100 and QS-PH6 will not work with it.

QuadStar can be an effective LAN for many companies or work groups. The cost is approximately \$500 per node and that's it. There are no extra options to buy. Check out QuadStar if you have a small- to medium-sized LAN in mind. It's just what the consultant ordered. §

*George Miller is a network systems analyst based in New Jersey with an interest in LANs, high-performance computers, and graphic environments.*

## Product Information

QuadStar Starter Kit with one QS-100 and QS-PH6	\$ 1,095
QS-100 Standard network adapter card	\$ 375
QS-188 High performance adapter card	\$ 475
QS-PH6, QS-100, plus 5 port passive hub	\$ 575
HUB-12 12 port active hub	\$ 795

### Quadram Corporation

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# Upgrading the XT

*Chip Replacement, Accelerator,  
Coprocessor & Motherboard Replacements . . .  
which to choose?*

by George Miller

**I**mproving the performance of an IBM PC, XT, or AT can be an exasperating and expensive proposition. There are many ways to change these machines into faster and more powerful microcomputers. Upgrading the AT with a replacement 386 motherboard or plug-in 386 card was discussed in the November/December 1987 issue of *Micro/Systems*. Here we will present three alternatives to upgrade an XT.

An XT's performance can be improved by swapping its 8088 processor for an NEC V20 (see *Micro/Systems*, November/December 1985) or increasing the clock frequency (see *Micro/Systems*, November/December 1986). However a change to an 80286 or 80386 processor is needed if you want to gain a substantial increase in performance or want to run one of the newer operating environments, such as OS/2, Windows 386, PC-MOS, or Concurrent DOS. In addition, these environments also typically require at least 1-2 megabytes (MB) of random-access memory (RAM). Let's take a look at the available upgrade alternatives.

## Processor Replacement

Replacing the 8088 processor chip is the simplest and lowest cost upgrade. This no-slot solution means removing the 8088 chip and replacing it with a new processor chip or

small adapter card that plugs into the processor socket on the motherboard. Such an upgrade can provide a 10 percent to 100 percent improvement in performance using a faster 8088 or NEC V20 chip and faster clock circuit. However, it provides no increase in functionality, such as the ability to run OS/2. By contrast, replacing the AT's 286 processor with a card containing only an 80386 usually provides no performance improvement but adds the needed functionality to run a more powerful operating environment, such as Windows 386. Processor replacement is the lowest cost upgrade but has many tradeoffs.

## Accelerator Cards

Accelerators cards are the next step up and can be divided into two types: souped-up processor replacements and mini-motherboards. Both approaches require removing the motherboard's 8088 and replacing it with a plug-in card and cable to the old 8088 socket. Processor replacement cards typically have cache memory to improve performance. The microprocessors on these cards tend to be 16-bit processors, such as an 8086, NEC V30, or 80286 for PC/XT-class machines. The cards provide major performance improvements, often as great as 300 percent. However, although the cards may have an 80286 on board, they

do not provide access to the extended memory required by OS/2.

The mini-motherboard cards provide all the parts normally found on the main motherboard, including the microprocessor, numeric coprocessor, RAM, and possibly the boot ROM and clock/calendar chip (as is the case with one of the cards reviewed here). The cards work like the processor replacement cards except that the onboard RAM provides better performance. These cards also tend to cost significantly more.

PC/XT mini-motherboard cards are popular because the 80286 chips on the cards work best with 16-bit memory. Putting memory on the card provides a way for the cards to access the extended memory required for more sophisticated operating systems, such as OS/2. However, providing extended memory on these cards does not guarantee OS/2 compatibility. 80386 mini-motherboard XT cards are now becoming available. AT mini-motherboard cards are all 80386-based. These cards tend to have 32-bit RAM to augment the AT's existing 16-bit RAM. The 32-bit RAM provides better performance while the 16-bit RAM provides a way to access more RAM than will fit on the card. Normally, there is a significant difference in performance between on-card and off-card memory. The 80386 cards provide support for

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80386 operating environments, such as PC-MOS. These cards tend to offer the most economical way to upgrade a machine to higher performance with more capabilities.

A special form of the mini-motherboard card, a "coprocessor board," retains the motherboard's microprocessor. Coprocessor cards operate in parallel with the motherboard's microprocessor, which is now relegated to I/O processing only. This approach provides better throughput but compatibility suffers because the coprocessor card does not have direct access to peripherals, such as video or floppy-disk cards. It is possible to have multiple coprocessor cards in a single computer, but these multiprocessor systems are limited to customized, special-purpose applications requiring custom programming or applications specifically designed for the coprocessor(s).

## Replacement Motherboards

Adding cards is fine if you have the slots and can deal with the remaining incompatibilities. Replacing the motherboard is the most compatible alternative. Both 80286 and 80386 XT motherboard replacements are available, including the two replacements reviewed here. Motherboard replacement offers one thing the other alternatives cannot offer; the ability to include wider bus card connectors. For example, an 80386 XT motherboard may contain 8-, 16-, and 32-bit connectors. This would allow an XT owner to install a 16-bit hard disk controller for higher performance. The previously discussed approaches would continue to use the old, slower, 8-bit, hard disk controller.

Which is best? That depends on what you want to pay and how much you want to change. The best low-cost solution for an XT is the processor replacement card which provides a faster processor but no access to extended memory. The more expensive alternative is the motherboard replacement. The price is on a par with the mini-motherboard cards,

but a completely new motherboard provides better compatibility and performance. Mini-motherboard cards are a reasonable approach and are easier to install than a motherboard replacement card. Coprocessors are the most specialized approach and should not be considered as a general system upgrade.

There are a number of companies that offer boards to upgrade your XT machine. A.I. Architects has its 386 coprocessor, the Hummingboard; AST Research recently started shipping the Xformer/286; and Intel is said to be coming out with an XT

version of its Inboard. What we offer here is a look at three upgrade alternatives that were among the first available: Wave Mate's Bullet 286e motherboard, Dyna Computer's SX386 motherboard, and Microsoft's Mach 20 enhancement board. Which board you choose will depend on your specific performance requirements and your budget.

*George Miller is a network systems analyst based in New Jersey with an interest in LANs, high-performance computers, and graphic environments.*

## The Bullet 286e Motherboard

by Roger T. Stevens, Ph.D.

**T**

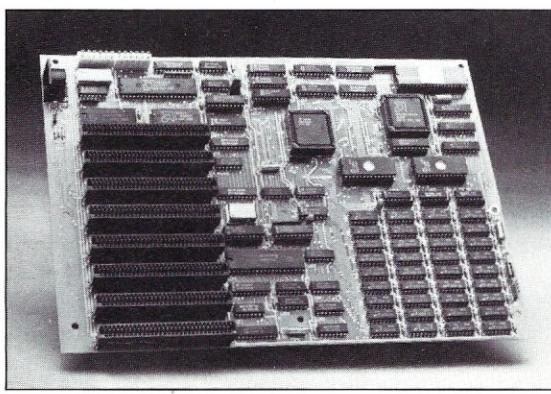
he Bullet 286e is an XT replacement motherboard using an 80286 microprocessor and one megabyte (MB) of memory. My benchmark tests show it to be faster than an IBM PC/AT. It is a well-designed and well-built unit which should offer trouble-free service.

### Installation

The instruction manual for the Bullet 286e goes into extensive detail on the installation procedure, but the process is so simple that one need only use common sense. First, unplug the external connectors and boards from the XT motherboard

and remove the disk drives and the screws or plastic fasteners securing the motherboard in place. Now remove the old XT motherboard and install the new Bullet board. I was pleased that the Bullet's power supply connectors were keyed so that the power supply plugs cannot be incorrectly inserted. Most PC-compatible power supplies have properly keyed plugs, but many clone motherboards use a single, inexpensive power connector that ignores the keying feature.

The switches and jumper options are now set, as explained in the manual; the disk drives are mounted; the plug-in boards inserted; and all connectors reconnected. The only problem I had was in connecting the speaker. The Bullet board uses pins 1 and 4 of the speaker connector and the instruction manual says this is compatible with the PC/XT, but the clone I have had a two-prong speaker connector. Thus, I had to do a little



rewiring. Other than that, the board worked perfectly on the first try.

I run the Bullet 286e with a California Digital combination floppy disk controller/real-time clock/serial and parallel I/O board, two Mitsubishi floppy disk drives, a JDR RLL hard disk controller board, a LaPine LT300 30 MB hard disk drive, a PC-Network 2 MB expanded memory card (populated with 512K), JDR EGA card and monitor, and a JDR PROM burner card. All work well with the Bullet 286e.

## Technical Features

The Bullet 286e uses a 7.15909-MHz clock. This has twice the color-burst frequency and half the dot-clock frequency required for the CGA board, thereby reducing the number of oscillators required and improving stability because there are no unsynchronized frequency signals floating around the board to cause problems. An internal 16-bit bus connects the microprocessor and memory. Fast memory is used with zero wait states for maximum speed.

Another improvement is the use of buffered outputs for all eight-card slots. The PC/XT buffers only the eighth slot; signal lines on the other seven slots are driven in parallel with some internal signal destinations. This reduces reliability, since a defective or poorly designed plug-in board can drop the strength of internal signals sufficiently to cause the system to stop operating or to have strange intermittent problems. With the Bullet 286e, all internal signals are isolated from the card slot drivers so that card problems have minimal effect upon internal operation. Furthermore, the signal timing to the card slots is designed to be compatible with the PC/XT, so there is no danger that the boards designed to work at the PC/XT's 4.77-MHz clock rate will be adversely affected by the faster Bullet 286e clock. A PAL-gate array provides bus transfer control and handles the non-maskable interrupt function for more sophisticated and reliable control than offered by the 8288 bus controller used in the PC/XT.

An added plus is a built-in hardware reset circuit—a two-pin connector located next to the keyboard connector for connection of a momentary switch. Also a connector supplies power for an LED "on" indicator and a pair of contacts for a keyboard lock switch, such as is used on the PC/AT.

## System Performance

The *PC Magazine* benchmarks (Table 1) demonstrate that in every case, the Bullet 286e is faster than an IBM PC/AT and much faster than an XT, Turbo XT, or XT equipped with an NEC V20 microprocessor.

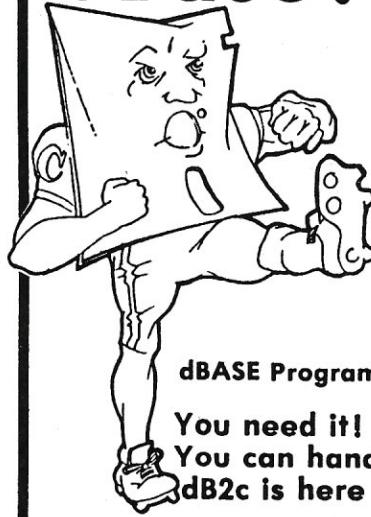
You would expect the IBM PC/AT to really shine on the hard disk test (Table 1) since it uses a 16-bit hard disk controller and a drive with a much faster access time than that used on the XT. Surprisingly enough, the Bullet 286e is the star due to the hard disk caching used on the Bullet board, but more about this later.

## Extra Memory? What For?

The Bullet 286e includes one megabyte of RAM. DOS can only directly use 640K of RAM. The remainder is assigned to displays, other I/O devices, and the BIOS ROM. The question then is why do you need this extra memory? It is not Lotus/Intel/Microsoft-compatible expanded memory or IBM extended memory. It is memory that replaces the system memory from 640K to 1 MB when a PHANRAM signal is sent to I/O port 0B0H. It can be accessed by the system but not by DMA (direct memory access). If you are doing assembly language programming, this additional memory can be used to generate larger programs and larger in-RAM databases. However, this is not an accepted convention since such programs would not run on some other machines. Also, if you don't return from the phantom memory to regular memory quickly and often, your display may go away.

The extra memory does have a use, however. The Bullet 286e ROM BIOS contains software that can use

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the extra memory for hard disk caching of read or read/write. The option is set by a pair of jumpers on the motherboard. The disk cache software traps interrupt 13H which controls disk I/O calls. Disk sectors are placed in the cache as required, and from then on calls to that particular sector only require interaction with the extra 384K of memory. When the cache memory is full and a sector is called for that is not in the cache, it is read from the hard disk into the location of the sector that has not been used for I/O for the longest period.

To test the caching, I wrote a short batch file that read the time, then transferred a 135K file from one hard disk directory to another three times, and then read the time again. With the caching disabled, the procedure required 20 seconds. With caching in use, the time dropped to 9 seconds the first time it was run and 6 seconds for succeeding runs. This is a substantial saving in hard disk access time, especially for repetitive tasks.

You also can use the extra memory as a RAM disk. Wave Mate has made P-Disk software available for the asking, a program that uses the extra memory as a 384K RAM disk. My copy of P-Disk arrived within a few days of my requesting it. It came with two pages of information on how to use the disk caching software and nothing about P-Disk.

The disk contains two programs: PDISK.BIN and PDISK.ASM. The first is a binary program. The second is a Microsoft .LST file showing both the full assembly language source and the assembled code. One could strip off the first 32 characters of each line, the page headings, and titles and end up with something that could be assembled with the Microsoft assembler.

It took me some time to solve the mystery, so to save you time here's what to do. First, rename the PDISK.BIN program as PDISK.SYS and load it to your system disk, then edit your CONFIG.SYS file to include the line:

DEVICE = PDISK.SYS

The software will then work perfectly, functioning in the same manner as any other virtual disk, and probably faster than most. I checked this software with some actual program runs and there were no problems. Thus you have two useful choices as to what you would like to do with your 384K of extra memory.

## Compatibility

Just as some XT programs will not run on a PC/AT, some programs will not run on the Bullet 286e. The instruction manual lists those programs known not to run, and provides a form for reporting programs that you find do not run. This goes into Wave Mate's list, but since they don't really offer to help you with incompatibility problems, the value of the report to the user is limited. Mostly, the types of programs that will not run are:

1. Programs requiring precise timing (e.g., COPY II and Copy-Write). These probably will not run on the PC/AT or Turbo XT.
2. Programs that check for the ROM IBM copyright notice (e.g., IBM demos and tutors). These probably will not run on any clone.
3. IBM BASIC and BASICA which must access the IBM ROM.

If you want to run BASIC programs, you will need GWBASIC or MBASIC. BASIC is supplied with many systems, such as the Compaq, Corona, etc. Many do not work with the Bullet 286e. Compaq BASIC Versions 2.0 and higher are on Wave Mate's list of programs that do not work for some unknown reason. I found that the Compaq BASIC will load and run programs that are typed in. However, when a program is saved to disk and then reloaded using the Load command, it loads and lists fine, but will not run. It has apparently corrupted part of the program memory, since when you type "Run," BASIC replies "Syntax error." Compaq BASIC Version 1.11 runs fine, however, although I haven't found out yet how to prevent it from insisting that it must be on

disk A or B.

## Future Compatibility

Microsoft will soon release OS/2 for 80286-based PCs. Will the Bullet 286e be compatible with this operating system? On the surface, there appears to be no reason why not. All of the machine language commands are there. Hopefully, if OS/2 will run on a PC/AT, it will run on the Bullet 286e as well. Or will it? Only time will tell.

I tried a simple test, the results of which offer some hope. DOS has an interrupt, 19H, which according to Peter Norton only works on the IBM PC/AT. This interrupt writes out a string on the display monitor at a selected location and in a selected color. I wrote a small program to utilize this interrupt and it ran on the Bullet 286e. Thus the Bullet's ROM BIOS is compatible with the IBM PC/AT, for this one instance at least. This is a good sign for the future.

## Subjective Impressions

Beyond actual physical checking and benchmark testing, there are some subjective impressions of a product that may be equally important. My first XT clone, for example, was a nice machine, but it occasionally generated a memory parity error that required me to start all over. Mostly, this was just a nuisance since I never lost any significant data. Also, when I filled the memory to 640K, it would no longer run Lotus 1-2-3 until I installed a new, corrected ROM BIOS. And my Turbo XT, just once, subtly corrupted some programs on the disk so that they would run, but never perfectly.

The Bullet 286e has given me absolutely no problems. It runs reliably day after day. Further, I am impressed with its detailed and easy-to-understand manual. I do not know about factory support; so far I have had no need of it, and if the system continues working as well as it has been, I may never find out.

## Conclusions

For about the same cost as an accelerator board, and for considerably less money than the cost of a new AT

clone, you can upgrade your PC/XT or XT clone to an 80286-driven machine that is almost completely compatible with the XT software and faster than an IBM PC/AT. In addition, there is an additional 384K of RAM that you can use as either a RAM disk or hard disk cache. The Bullet 286e makes upgrading an XT simple and the board is highly reliable.

*Roger T. Stevens is a systems engineer with the MITRE Corporation in Albuquerque, New Mexico. He received his doctorate in Electrical Engineering from California Western University.*

### Product Information

Bullet 286e	\$895
Single evaluation unit	\$599
OEM quantity	\$359

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## The Dyna Computer SX386 Motherboard

by Stephen M. Leon

**T**he Dyna Computer SX386 motherboard enables a PC/XT or XT clone to be upgraded to the Intel 80386 32-bit microprocessor, providing processing speed equal to that of IBM or Compaq 386 systems. However, note that its price, as well as some other shortcomings, may make you question such a move.

Don't get me wrong. The product works, and for the most part works well and its numbers are impressive. Except for a clock that could not keep time, it ran flawlessly.

It is relatively simple to replace the motherboard in an XT with a Dyna 386. First, remove all the plug-in cards, unplug the power supply connectors, remove one screw, slide the motherboard to allow the plastic separators to release, and lift the board out of the case. Then transfer the plastic separators to the SX386, slide the board into place, and rein-

stall the screw, power supply connectors, and plug-in boards.

I've installed many an XT motherboard. The first time I "fried" the board because I did not know the trick "black-to-black in the center" for the two power supply plugs. Once I knew that technique, I never again ruined a board. The Dyna manual describes this sensitive process as follows:

"The SX386 system is designed to be assembled like a standard XT computer. . . . Once the SX386 has been installed in the chassis, and the power supply, battery, and keylock panel connectors have been mated, the adapter cards may be installed."

For an additional \$200, Dyna will install its board in your machine for

you. However, don't expect any installation help from the manual. If you don't know what you are doing, it can cost you a \$1,650 board.

If you purchase the Dyna SX386, you are in for some surprises. First of all, you can't use your XT keyboard; you must use an AT keyboard. Unless you happen to have a convertible XT-AT keyboard, plan on spending an additional \$100. Then there is the power supply. The Dyna SX386 requires a minimum of 145 watts to operate. The clone in which I installed the board had a 150-watt power supply, but the IBM PC/XT and most XT compatibles have only 130- or 135-watt power supplies. Therefore, you may also need a new power supply. If so, add another \$65 to the overall cost.

What about floppy drives and hard disks? Dyna recommends a 1.2-megabyte (MB) drive. However, a 360K drive and an ordinary floppy controller work fine. Thus, the XT's floppy and controller can be used.

But what about your hard disk? Do you really think you will be satisfied running along at 16 MHz with a 90+ millisecond XT hard drive with an 8-bit controller? You may wish to replace the 8-bit XT hard disk controller with an AT-type, 16-bit controller. However, you will find that the standard AT hard disk controller is too tall to fit in an XT case. The only disk controllers you can use are the low-height, hard disk/floppy controllers designed for the IBM PC/XT 286. And it is unlikely that a 16-bit RLL or any of the newer, more sophisticated controllers will work with the Dyna 386.

The Dyna 386 came with a 15-page manual and a "CMC 386 System User's Guide." The board arrived with a broken keyboard connector, but the system worked despite the broken connector. It came with 2 MB of 100-nanosecond memory on the board. This can be expanded to 8 MB on the motherboard at \$270 per megabyte. The

board has a slot for an 8- or 10-MHz 80287. It comes with four 16-bit AT-compatible and four 8-bit XT-compatible slots.

Before installing the board, I had to go to Radio Shack and buy a battery case for four AA cells and solder a plug to attach the battery to the board. It took only minutes to take the old components out of my XT clone, change the motherboard, and install the Dyna 386. Fortunately, I had a copy of the IBM PC/AT Advanced Diagnostics. Dyna does not supply a basic setup program and such a program is needed to setup the computer. Dyna supplied very little. I even had to provide my own jumper to set the machine up for a color card.

The only instructions on using the Advanced Diagnostics Setup program for this machine were in the "CMC" manual, and those instructions were wrong. For example, the manual does not tell you that when you use an 8-bit, hard disk controller

**Table 1. PC Magazine Benchmark Tests V3.0 (all times in minutes:seconds.tenths of seconds)**

	Bullet 286	Dyna 386	Mach 20	IBM PC/AT	AT Clone 8 MHz 0 Wait	Turbo XT Clone	XT Clone NEC V20	PC XT Clone
<b>Test</b>								
1. NOP Executions Spanning 128	4.72	2.09	13.00	5.60	4.23	6.10	10.16	10.22
2. Do-Nothing (1 NOP) Loop	3.63	1.81	3.00	4.94	2.97	5.93	9.17	9.94
3. Integer Add from Memory Loop	2.14	0.88	2.20	2.97	1.87	5.93	9.06	9.94
4. Integer Multiply from Memory Loop	1.32	0.55	1.50	1.65	1.10	5.99	5.44	10.05
5. Floating Point without coprocessor	36.30	15.49	35.10	46.70	27.30	93.80	133.30	157.10
Prime Numbers 1-16384 (25 repetitions)	12	5	5.4	19	10	34	55	57
<b>Memory Test</b>								
1. Memory Read	1.10	.71	1.4	1.81	.93	3.57	3.57	5.99
2. Memory Write	1.10	.71	1.4	1.76	.93	3.63	3.57	5.99
<b>Norton System Index (SI)</b> (Performance relative to IBM PC)								
	6.6	15.3	7.34	4.8	8.3	1.66	1.7	1.0
* Tested with Miniscribe 3425 hard disk.								
** Tested with high speed Seagate 4096 hard disk								
n/a Results not available for valid comparison								

instead of a 16-bit controller you must tell the diagnostics program that there are "no hard drives." Additionally, while the Dyna has 2 MB on board, the only configuration the machine would accept was 640K of basic memory and 1024K of expanded memory. Don't look for the answer to that one in the documentation either.

There are 40 separate items that can be configured. The only thing the manual tells you about these items is that the wrong combination could lock up the system. You then have to disconnect the battery and wait 10 minutes for the CMOS to lose the configuration before trying the next setup combination.

You can enable or disable "shadow RAM."<sup>1</sup> Enabling it should speed access time to the BIOS. If you have an EGA, you can also put the EGA BIOS into shadow RAM for extra speed. Whichever choice you make, the machine comes up with the statement "Shadow RAM Enabled"—annoy-

ing, but you could live with it. However, you could not live with the fact that, notwithstanding what the manual says, you can not slow the processor down from 16 MHz to 8 MHz. As a result, the machine would not run any copy-protected software. While most large software companies have abandoned copy protection, you could not use this machine for protected vertical-market programs.

### Factory Support

I called Dyna twice and got through without any wait. The first time, I was told that, since the board I had came with an American Megatrends Inc. BIOS instead of the Phoenix or Award BIOS promised in the documentation, they were not sure what was or was not supported. My second call brought the promise that they would send me a replacement PROM immediately to solve the problem. It never arrived.

The 80386 chip was marked for

16-bit operation only. I ran a 386 test program available on my BBS and confirmed that the Intel 386 chip was defective. This meant that it might not run OS/2. I called Dyna and was told that as soon as the 32-bit chips were available, purchasers could return the 16-bit chip and Dyna would replace it. This information was nowhere to be found in the paper work. Additionally, there was no mention of any warranty. In fact, I had to find the company's phone number on the invoice, not in the documentation.

With all the bad news about the product, the numbers were good. On Norton's SI Version 3.10 the Dyna 386 came up with a rating of 15.3. My 8-MHz, 0 wait state, AT clone has only an 8.3; and my Turbo XT clone has an SI of 2.9. The numbers are thus better than a Compaq 386, and at a far lower price.

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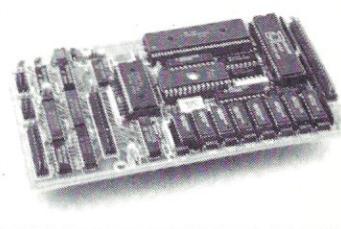
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<sup>1</sup> Shadow RAM is a technique to speed up access to the system BIOS by transferring the BIOS from the slow-access BIOS ROM into fast-access RAM at boot time. Then all BIOS accesses are made from the faster RAM copy with an improvement in throughput.

*Stephen M. Leon is a lawyer and an active participant in the writing and distribution of public domain software.*

## Product Information

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# The Microsoft Mach 20 Board

by George Miller

**T**he Mach 20 is Microsoft's answer to upgrading a PC or XT. This card supersedes the old 8086-based Mach 10 card, which was needed to make Windows fly on 8088-based machines. Windows 2.0 can now be effectively used on a PC or XT, but the 80286-based Mach 20 board really makes a difference. In fact, the Mach 20 can turn an old PC or XT into an AT-class machine, not just a faster PC. This means OS/2 compatibility is available, too.

The Mach 20 actually has two add-on daughter boards. One is a floppy disk controller card (the Mach 20 Disk Plus); the other is a memory card (the Mach 20 Memory Plus) that provides from 0.5 to 3.5 megabytes (MB) of memory as either extended or expanded random-access memory (RAM). The latter is compatible with the new EMS 4.0 specification, including full support for all the 4.0 features. The base card provides an 8-MHz, 80286 accelerator with the Microsoft InPort for a Microsoft mouse (not included). At \$495, this card is a reasonable accelerator in its own right. The \$395 memory card must be added for ex-

tended memory support. The floppy disk controller is only \$99. The advantage of a new disk controller is support for the 1.44-MB, 3½-inch floppy disk drives.

The construction of a fully loaded system looks like a Chinese puzzle. The accelerator card starts out as a half card. The floppy disk card plugs into the side of the accelerator card making it wider while a connector on the back is for the memory card. Adding the memory card makes the whole system into a full-length card. This may sound flimsy but it is quite rigid and rugged. It does fill up the slot, though.

The floppy disk and mouse options make it possible to put the Mach 20 into just about any system that is completely full by pulling the floppy disk or mouse controller card that may already be in the computer. A completely full system with no mouse and a combination floppy/hard disk controller may make life a little more difficult because something will have to be removed to make room for the accelerator card.

Although there may be some concern that Microsoft is a relative new-

comer to the 80286 accelerator board market, there is no need to worry. The card was put together with the help of Personal Computer Support Group, the same company that makes the popular Breakthrough 286-8 and 286-12 accelerator cards. (Just look on the Mach 20 circuit board for the initials.) This union has resulted in an even better product in the Mach 20.

## Installing the Mach 20

Putting the Mach 20 into a PC is similar to installing any other accelerator board. The 8088 is removed and replaced by a cable that connects to the Mach 20 board, which itself board contains number of jumpers for setting the cache options and mouse interrupt. The documentation is clear as to the settings and options available. The Mach 20 is easy to install because it is a half card. The memory and floppy disk controller must be installed before the card is put into the PC. The main problem is that the 8088-socket-to-Mach 20 cable length is limited so the closer the board is located to the 8088 socket the better. Having separate floppy disk and hard disk controller cards will make installation more difficult since the disk cables have been moved, but it is possible and patience is all that is needed. Switching cables from an existing floppy disk controller to the Mach 20 disk controller actually makes the job easier.

The Mach 20 memory addition precludes the use of other memory on the motherboard and any EMS RAM cards that may be installed. However, the memory chips from these cards can usually be moved to the memory addition card. If the card memory is part of a multi-function board, then the RAM can be moved, the memory support disabled, and the other peripheral support retained.

Checking out an installed Mach 20 also is relatively easy; either it works or it doesn't. Checking out the cabling and card jumpers usually fixes things. If all else fails, take out the Mach 20, pop in the 8088 and call

Microsoft. The staff is very helpful, once you get through on Microsoft's support line.

## Performance

The performance of the Mach 20 varies depending upon its configuration and the associated peripherals installed on the PC. The Mach 20 without the memory addition runs about 60 percent to 80 percent the speed of an 8-MHz IBM PC/AT. The main problem is that although the Mach 20 memory cache is efficient, eventually an access must be made to the 8-bit memory found on the motherboard or a non-Mach 20 memory board.

Including the Mach 20 memory card makes a major difference. The Mach 20 plus memory card has essentially the same performance as an 8-MHz IBM PC/AT. Most peripheral adapters work at about the same speed, too, because they tend not to be limited by the bus bandwidth. Memory, hard disk controllers, and specialized coprocessors (e.g., graphic coprocessors) are the exception. A wider bus and higher bandwidth always helps, which is one reason to add the Mach 20 memory addition. The Mach 20 floppy disk addition has little effect because of the limitations of a floppy disk.

Coprocessors are of little consequence since the Mach 20 provides no possibility for adding 16-bit, AT-compatible cards. Hard disks, on the other hand, can improve their performance through the use of disk caching programs. The Mach 20 works well with its disk caching program and the effective performance of an XT's hard disk can be improved. However, it will not be the same as an AT's hard disk. The disk caching program works with EMS memory, provided either by the Mach 20 memory addition or an EMS memory card such as the Intel Above Board. If better performance is needed, a second hard disk can be added with a faster seek time. The main problem is that the XT's hard disk controller performance cannot be increased and the data transfer rate of the disk cannot be changed.

Moving up to a real AT or going to a new motherboard that supports a 16-bit disk controller is the only way to match an IBM PC/AT.

The Mach 20 also performs well when an 80287 is installed since it runs on the same 16-bit internal bus as the 80286. There is no difference between it and an AT because, with the Mach 20 memory addition installed, floating point data is loaded from and stored to 16-bit memory.

## Compatibility

The Mach 20 will be compatible with OS/2 when Microsoft supplies it. The main limitation will be the amount of extended memory. The Mach 20 is not capable of handling 6 MB of extended memory at this time. However, it might be a good idea to look into a machine with greater capability if you need that much memory. The Beta version of OS/2 which is already available will not run on the Mach 20, but it also doesn't run on a PS/2 machine. Minor customization will be necessary, but Microsoft will undoubtedly provide it in due time.

Most AT-compatible programs will run with the Mach 20. The main missing link is high-density floppy disk drives because most applications destined only for AT-class machines are distributed on 1.2-MB floppy disks. Luckily, the Mach 20 floppy disk controller addition handles this type of drive and you may want to buy one along with the Mach 20.

Most PC-compatible products work with the Mach 20, but two types of programs cause problems. The first are copy-protected programs. Luckily these tend to be following the dinosaurs and alternative, non-copy protected programs are usually available. The second type of problem are communication programs. Early versions of Crosstalk will not work when the Mach 20 cache is turned on because the 80286 runs too fast. Turning the memory cache off, which can be done under software control, causes the Mach 20 to run at about 8088 speeds and allows programs like Crosstalk to run on the Mach 20 without modification.

Fortunately, most programs, including Crosstalk, have patches available that allow the programs to run at AT speeds. Most current programs have been written so that the speed difference is not a problem.

The Mach 20's ability to switch from full speed to 8088 speed should let you run your existing programs as they run now or possibly faster. Trial-and-error is the only real test, but the Mach 20 should prevail well over 90 percent of the time.

## Summary

Microsoft has a real winner here. The Mach 20 is one of the few products that can claim that it will run OS/2 software without reservation. The modularity of the product also provides an upgrade path. Today, start with the accelerator card only for more speed. Tomorrow, upgrade to the memory board when you need EMS or if you want to move up to OS/2. Add the floppy disk card if you need another slot or if you want to use a 1.44-MB, 3½-inch floppy disk drive.

The total price for all three pieces is just under \$1,000; about the same price of most other XT upgrade solutions. And Microsoft products are usually heavily discounted. The Mach 20 does offer two things the others do not: incremental expandability and Microsoft support. If you can afford the upgrade and have the experience, go with a new motherboard. If not, consider the Mach 20; it's a solid product. §

*George Miller is a network systems analyst based in New Jersey with an interest in LANs, high-performance computers, and graphic environments.*

## Product Information

### Mach 20 Performance

Enhancement Board	\$495
Mach 20 Memory Plus	\$395
Mach 20 Disk Plus	\$ 99

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# All About dBASE

*This is the first of a series of columns that will provide tips and techniques for implementers of database software on the PC. Reader suggestions, comments, and questions are encouraged.*

*In addition to his credits which appear at the end of this column, P. L. Olympia is the sysop of the Darwin BBS in Gaithersburg, Maryland; (301) 251-9206. His BBS supports database programmers and LAN system integrators.*

In this column, I'll cover the entire dBASE landscape, including tips and techniques in using dBASE, compatible compilers, and related products. Most of the time, I'll use the term "dBASE" in the generic sense (forgive me, Ashton-Tate) to include FoxBASE+, Clipper, Quicksilver, Front Runner, and Force III. I'll also describe how to create and use tools that extend the power of dBASE, as well as how to extract useful information from the format of dBASE files, information that the manual doesn't give you.

Naturally, I also intend to discuss burning issues of the day, for example, the raging debate about a language standard for dBASE, and the work of the Standards Committee, which has representation from almost all vendors except Ashton-Tate. Should the standards specifications come from competing vendors

or should they come from the grassroots of dBASE users? As I write this, some of us are hatching plans to establish a National dBASE Users Group, partly to help ensure that your voice is heard above the din of this debate.

## Quick Reviews

From time to time, I'll review products, public domain or commercial, of interest to dBASE users everywhere. Ironically, some of the products which dBASE users find to be the most useful have nothing to do with dBASE *per se*. Take CTRLALT, for example. This marvelous public domain program written by Barry Simon and Richard Wilson is a memory-resident program that, in my view, is the closest thing to a Programmer's Swiss army knife (and very compact at that). For starters, this program has many pop-up tables, including ASCII, hex, attribute, and color. It gives you the scan code of any key you press. If you are a dBASE II programmer, you will find the hex table useful in writing programs that use Peek and Poke.

CTRLALT is a handy tool for adding graphic characters and boxes, not only to any dBASE menus and screens you design but also to documents you write. While its ASCII table is on display, CTRLALT lets you pick off one or more characters from the table and insert those into the screen or document on which you are currently working. Its cut-and-paste facility is ingenious and easy to work with. You have the option of including or removing a carriage return/linefeed (CR/LF) sequence at the end of each line that you "cut."

When you "paste" the lines you've cut, you have a choice of a fast or slow insert mode to accommodate programs that cannot handle a fast keyboard.

CTRLALT provides complete support for a dual-monitor system. It also gives you the facility to send control codes to your printer to change its print mode. And since CTRLALT is in memory at all times, you need not exit whatever program you're currently working on just to reset the printer.

The one feature of CTRLALT that has saved me countless hours of agony is its ability to bring back DOS in situations when the machine seemed to hang so high that the only apparent alternative is to reach for the big red switch. You know the predicament only too well. You are testing a new program and suddenly your keyboard locks up; you have important data stored in your RAM disk; and if you power down now, all that data will just go to silicon heaven. What you wouldn't give to just have a few seconds to save the data to a real disk! What to do? Reach for CTRLALT.

It happened to me again just this morning. (If you are a FoxBASE+ user you'll be interested in this story.) I had a FoxBASE+ compiled program that ran on a LAN subdirectory under FoxBASE+ multiuser runtime. When I copied everything to a local hard disk and ran the program from there, the machine hung instantly. However, if I used the interpreter rather than the run-time version, the program worked flawlessly. It seemed to be a bug in the run-time version, but I wasn't quite ready to jump to that conclusion. To investigate the source of the problem would require a lot of trial and error, repeated machine lock-ups, and inevitable reboots; that is, if I didn't have CTRLALT. I soon found that the program would run if I didn't have the configuration file, CONFIG.FX. Clearly, there had to be a set parameter statement in that file that the FoxBASE+ runtime thinks is fine on a LAN subdirectory but not on a local disk. I proceeded to comment out each statement in the file

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and used CTRLALT to bring back DOS each time the machine appeared hopelessly hung. As it turned out, the offending statement was:

**EXCLUSIVE = OFF.**

FoxBASE+ runtime will not allow you to use a database resident on a local hard disk unless **EXCLUSIVE = ON**, which is the default state.

CTRLALT is a 3K executable file that uses less than 7K of RAM. It

comes with the assembly language source and outstanding on-disk documentation. It, like all other public domain and shareware programs I will describe here, is available from most bulletin board systems, including my Darwin BBS.

### **dBASE File Recovery**

Reconstructing damaged dBASE files is becoming a hot issue again. Damaged files are caused, more of

ten than not, by user carelessness. (Consultants just love to blame users, don't they?) Most of the damaged files I've had to reconstruct became damaged when users simply power down the computer when they leave their desks without giving dBASE a chance to flush its buffers and close its files. Of course, the length of time that a dBASE file is open in a typical application system only helps to compound the problem.

When a system shows signs of file damage, the culprit may be corrupted index files rather than damaged DBF files. A corrupted index file is indicated by error messages such as "EOF encountered" or "Record out of range." The preferred way to rebuild the index file is not to use the REINDEX command but rather the INDEX command where the key expression is specified again. REINDEX assumes, although not always correctly, that the key expression stored in the index file header is undamaged. Clearly, if the file header is corrupt, no amount of REINDEX will correctly rebuild the index file.

The ever-present possibility of index file corruption should be taken into account in applications coded using dBASE-compatible compilers. It is always good practice to include a function for rebuilding index files in every compiled application. The problem is less severe with Quicksilver, which maintains complete file compatibility with dBASE, since the index files can always be rebuilt using dBASE. It is most severe in FoxBASE+ Runtime and Clipper Autumn '86 version, where the user does not have the ability to rebuild index files without a utility function or program. Note that the Clipper Summer '87 version (presumably released by the time you read this) will give you a choice of dBASE or Clipper index file formats.

The most common type of dBASE file damage is corruption of the database file (DBF). Typical DBF problems include damaged header records, shifted data and embedded end-of-file (EOF) characters, or nulls in the file. A file with a corrupted

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header record is one that dBASE may no longer recognize as its own (the dreaded "not a dBASE III file" message, guaranteed to get your adrenalin going), or one where the DBF structure definition is scrambled or gone. Embedded EOF characters also generate the "EOF encountered" message. In a file with shifted data, parts of one field or record spill over into the next.

In 1984, I wrote a public domain program called DB3FIXPO, which has since served me and many others well in recovering damaged files with corrupted headers or shifted data. DB3FIXPO is primitive compared to a new program code-named TIE (short for Take It Easy), the best dBASE file recovery program I have seen so far.

TIE is very easy to use and takes a visual approach to data recovery. You can shift data by bytes, records, or clusters; automatically find good records; pull any good records anywhere on the disk; and adjust the DBF structure definition to fit the data. Naturally, it can also rebuild the DBF structure. TIE is a commercial program that is likely to be renamed when it is released in the near future. It is the only dBASE file recovery software you'll need. I recommend it highly.

TIE was written by Keith Mund of Ashton-Tate. Keith is the same smart fellow who wrote SAY2FILE, a public domain program that redirects the output of the dBASE @ .. SAY command to a file. I use this program to capture screens of dBASE applications for inclusion in the system documentation and for making slides for use in training seminars.

### And Now A Few Techniques

In the course of debugging a program, you are always faced with temporarily disabling (commenting out) a block of code. The usual approach is to turn each line into harmless comment by adding an asterisk at the beginning of each line. Then, when you are done debugging, you modify each line again by removing the asterisk. That's a lot of unnec-

essary work.

All you really need to do is surround the block of code with an IF .F.-ENDIF pair, like this:

```
IF .F.
  * All executable
  * statements inside
  * this block are
  * disabled
  ... statements ...
ENDIF
```

Then, you just need to remove (or comment out) the IF-ENDIF pair if you want the block of code to be executable again. Of course, you may also use DO WHILE .F. instead of IF .F. (and ENDDO to terminate that instead of ENDIF).

I use this technique to include extensive documentation, including revision history, file structures, index expressions, and work-area descriptions, at the beginning of each pro-

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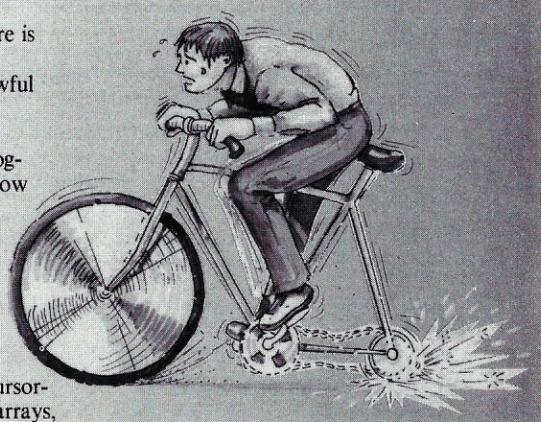
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**Listing 1. A turbo program using I/O routines.**

```

procedure setup_registers;
inline($eb/500);
begin
  $22/$41/stack_seg/ [mov ax,cs:stack_seg]
  $82/$DD/ [mov ss,ax]
  $22/$41/data_seg/ [mov ax,cs:data_seg]
  $82/$DD/ [mov ds,ax]
  $22/$41/extra_seg/ [mov ax,cs:extra_seg]
  $82/$CD/ [mov es,ax]
end;

{reset 8259 masks}
port[$21]:=mask1 $259;
inline($eb/500); {delay}
port[$21]:=mask2 $259; {delay}
{When this procedure returns, it will return to the place where
 goto real was called from. errorflag set by fault handlers.}
if errorflag then halt;
end;

procedure save_segs;
{Saves the current segment values in typed constants so they can
 be retrieved when program returns from protected mode.}
begin
  data_seg:=ds;
  extra_seg:=es;
  stack_seg:=ss;
end;

procedure save_8259_regs;
{Saves current 8259 masks so they can be replaced on return to
 real mode.}
begin
  mask1 $259:=port[$21];
  mask2 $259:=port[$41];
end;

procedure set_cmos_for_shutdown;
{sets cmos ram so that the reset that brings this program back to
 DOS jumps to the correct address in this program.}
begin
  port[$70]:=$0F;
  port[$11]:=$00; {delay to make sure output finished, as in BIOS}
  inline($eb/500); {delay}
end;

{the following routines are the entrance points for all of the 80286
 faults. The inline code is used to load DS and SS to known values
 before branching to the standard error handling routines. This avoids
 a second fault if DS and SS contain junk.}
procedure fault0;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault0:=$18;fault0;
procedure fault1;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault1:=$18;fault1;
procedure fault2;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault2:=$18;fault2;
procedure fault3;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault3:=$18;fault3;
procedure fault4;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault4:=$18;fault4;
procedure fault5;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault5:=$18;fault5;
procedure fault6;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault6:=$18;fault6;
procedure fault7;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault7:=$18;fault7;
procedure fault8;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault8:=$18;fault8;
procedure fault9;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault9:=$18;fault9;
procedure fault10;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault10:=$18;fault10;
procedure fault11;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault11:=$18;fault11;
procedure fault12;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault12:=$18;fault12;
procedure fault13;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault13:=$18;fault13;
procedure fault14;begin:inline($b8/$18/$8e/$d8/$b8/$28/$8e/$d0);
fault14:=$18;fault14;

procedure setup_idt;
{This procedure loads the idt with the appropriate values to handle
 all 80286 processor faults and BIOS rtrns needed by turbo.}
var x:integer;
begin
  {The first 14 selectors are all 80286 faults, and are directed to
  fault handling routines.}
  for x:=0 to idt_size do
    set_idt_desc(x,0,0,0);
  set_idt_desc($18,ofs:fault0)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault1)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault2)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault3)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault4)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault5)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault6)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault7)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault8)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault9)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault10)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault11)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault12)+7,code_desc,0,$86;
  set_idt_desc($18,ofs:fault13)+7,code_desc,0,$86;
  set_idt_desc($10,video_ofs,video_desc,0,$86); {bios code gates}
  set_idt_desc($15,cassette_ofs,bios_desc,0,$86);
  set_idt_desc($21,keyboard_ofs,bios_desc,0,$86);
  set_idt_desc($21,tick_ofs,bios_desc,0,$86);
  set_idt_desc($60,timer_int_ofs,bios_desc,0,$86); {hdwr interrupt gates}
  set_idt_desc($61,kbd_int_ofs,bios_desc,0,$86);
end;

procedure addr24(segment,offset:integer; var a24w:integer; var a24b:byte);
{To add to protected mode, physical address must be expressed
 as 24 bit value. This routine takes the lower 8 bits of a24
 bit address in a24w, and puts the upper 8 bits in a24b.}
var x:integer;byt:byte;
begin
  $8B/$86/segment/ [mov ax,segment][bp]; move segment over 4 bits
  $80/$10/$00/ [mov dx,16];
  $01/$8E/offset/ [mul dx,16];
  $01/$8E/offset/ [add dx,offset][bp]; add offset and send
  $83/$D2/$00/ [adc dl,0]; carry bit to dl
  $88/$96/Y/ [mov y[bp],dl]; save result
  $83/$88/X/ [mov x[bp],ax]; save result
  a24w:=x;
  a24b:=y;
end;

procedure setup_gdt;
{This procedure sets up the GDT with the descriptors required by
 Int 15, function 89. Other descriptors are set as needed.}
var a24w:integer; a24b:byte;
begin
  set_gdt_desc(0,0,0,0,0); {Function
  {0 dummy descriptor}
  addr24($e6,ofs:gdt),a24w,a24b); {1 GDT alias}
  addr24($e6,ofs:(idt),a24w,a24b); {2 IDT alias}
  set_gdt_desc(2,size_of(idt),a24w,a24b,$92); {3 Data descriptor}
  addr24($e6,ofs:(a24w,a24b),a24w,a24b,$92); {4 Extra descriptor}
  addr24($e6,ofs:(a24w,a24b),a24w,a24b,$92); {5 Stack descriptor}
  set_gdt_desc(5,$ffff,a24w,a24b,$92); {6 Code descriptor}
  set_gdt_desc(6,$0000,a24w,a24b,$92); {7 Temp Bios CS}
  addr24($40,$0200,a24b,$92); {8 bios data segment $40}
  addr24($50,$0000,a24b,$92); {9 video segment $50}
  set_gdt_desc(10,$1000,a24w,a24b,$92); {10 Dos data segment $50}
  addr24($e6,seg_0,a24w,a24b); {11 Video segment for EGA}
  addr24($b000,$0200,a24w,a24b,$92); {1600 mono display buffer}
  set_gdt_desc($1600,$4000,a24w,a24b,$92); {1700 CGA display buffer}
  addr24($b800,$024w,a24b,$92);
  set_gdt_desc($1700,$4000,a24w,a24b,$92);
end;

procedure protected_mode_exitpoint;
{When program returns to real mode, if comes here.}
begin
end;

procedure setup_return_addr;
{Sets up the approp BIOS memory location with the address of the
 code to be jumped to upon return from the real mode.}
begin
  memw[$0040:$67]:=ofs(protected_mode_exitpoint)+7;
  memw[$0040:$69]:=cseg;
end;

procedure goto_protected;
{Takes 8286 to protected mode.}
begin
  errorflag:=false;
  save_8259_regs;
  save_segs;
  set_cmos_for_shutdown;
  setup_return_addr;
  {DO NOT use Turbo. interrupt procedure here since BIOS kills BP.}
  inline($eb/500); {delay}
  $88/$d8/ [mov ax,ds]; {load address of GDT into es:si}
  $88/$Sc/ [mov es,ax];
  $88/$70/ [mov si,ds]; {gdt}
  $83/$70/ [mov ah,60]; {bh,b1 contain new location for}
  $84/$89/ [mov ah,89h];
  $80/$21/ [int 13h];
  port[$42]:=$Ffc; {changes int mask to allow kbd and timer ints.}
  inline($eb/500); {delay}
end;

procedure do_tests;
{sample code that demonstrates protected mode operation of I/O rtrns.}
var linstring[$80]:xinteger;
begin
  procedure test_screen_io;
  {test clrscr, gotoxy, writeln.}
  begin
    clrscr(5,5);
    writeln('WELCOME TO PROTECTED MODE!..');
    writeln;
  end;

  procedure test_keyboard_io;
  {test readin}
  begin
    writeln('Enter your name: ');
    readin(ln);
    for x:=1 to 5 do
      writeln(' ',ln);
    writeln;
  end;

  procedure test_disk;
  {test disk I/O}
  var xtext:xinteger;
  begin
    goto real;
    writeln('Switched to real mode.');
    assign(f,'xxx.xyz');
    rewrite(f);
    writeln('writing to file.); writeln;
    for x:=1 to 10 do
      write(f,'Hello');
    close(f);
    writeln('switching back to protected mode.');
    goto_protected;
  end;

  begin
    {goto protected mode and do tests.}
    goto_protected;
    test_screen_io;
    test_keyboard_io;
    test_disk;
    goto_real; {BE SURE to return to real mode before exiting.}
  end;
end;

procedure get_int_routine_addrs;
{Get all BIOS and hardware interrupt routine addresses needed to
 fill IDT.}
begin
  result.ax:=$3510; {function $35=Get vector. $10 is vect to get}
  intr($21,result.ax); {call DOS function $35. get vector 10 (video)}
  video_ofs:=result.bx;
  video_desc:=result.es;
  result.ax:=$351a;
  intr($21,result.ax); {call DOS function $35. get vector 1A (timer)}
  timer_ofs:=result.bx;
  result.ax:=$3508;
  intr($21,result.ax); {call DOS function $35. get vector 8 (timer int)}
  timer_int_ofs:=result.bx;
  result.ax:=$3516;
  intr($21,result.ax); {call DOS function $35. get vector 16 (keyboard)}
  keyboard_ofs:=result.bx;
  result.ax:=$3514;
  intr($21,result.ax); {call DOS function $35. get vector 9 (kybd int)}
  kbd_int_ofs:=result.bx;
  result.Xx:=$351c;
  intr($21,result.ax); {call DOS function $35. get vector 1C (user tick)}
  tick_ofs:=result.bx;
  result.ax:=$3515;
  intr($21,result.ax); {call DOS function $35. get vector 15 (cassette)}
  cassette_ofs:=result.bx;
end;

procedure handle_ega;
{replaces EGA bits with standard AT bios code. You must find
 the correct address for this code on your AT.}
begin
  result.ax:=$3510; {$35 in AH requests "get vector" function}
  intr($21,result.ax); {call DOS function $35}
  ega_ofs:=result.bx;
  ega_seg:=result.es;
  result.dx:=result_ax; {this code}
  result.dx:=$3605; {**** address of int 10 code in your AT's ROM.}
  result.ds:=$0000;
  result.ax:=$2510; { $25 in AH requests "set vector" function}
  intr($21,result); {call DOS function $25}
end;

procedure fix_back_ega;
{sets bios back to use EGA's code.}
begin
  result.dx:=ega_ofs;
  result.ds:=ega_seg;
  result.ax:=$2500; { $25 in AH requests "set vector" function}
  intr($21,result); {call DOS function $25}
end;

function OK:boolean;
var ch:char;
begin
  ch:=in;
  writeln;
  writeln('TURBO PASCAL PROTECTED MODE DEMONSTRATION');
  writeln('Marshall Brain 1/20/86');
  writeln('If your computer contains an EGA card for the display, you need');
  writeln('to modify this program before it will run on your system. The');
  writeln('instructions and reasons for this modification are contained in');
  writeln('the EGA sidebar of this article. Press "Y" to continue execution');
  writeln('or "N" to abort. ');
  read(kbd,ch);
  if ch in ['Y','y'] then OK:=true else OK:=false;
end;

begin {main routine}
  screen_check;
  if OK then
    begin
      handle_ega; { }
      get_int_routine_addrs;
      setup_idt;
      do_tests;
      {fix_back_ega; { }
      writeln;writeln('Program complete. Back to real mode.');
    end;
end;

```

gram—all without having to use a single asterisk. For example,

```
IF .F.  
  MIPSMAIN.PRG  
  by -p.o.-  
  Revision history:  
  ....  
  DBFs used, structures  
  and work area:  
  ....  
  NDX files and key  
  expressions  
  ....  
ENDIF
```

The technique also is useful when you want to protect a block of code from Clipper. Everyone knows that, theoretically, you can force Clipper to ignore a set of statements by surrounding it with IF CLIPPER-ENDIF. Everyone also knows that, sometimes, Clipper insists on parsing commands inside that block, resulting in irrelevant diagnostic messages. The solution is to use the TEXT-ENDTEXT pair inside the IF .F. block. For example,

```
IF .F.  
  TEXT  
    commands here are  
    free from Clipper  
    parsing  
    ... statements ...  
  ENDTEXT  
ENDIF
```

## Speeding Up Your Code

Most people will tell you that you can speed up your dBASE code by removing comments, abbreviating commands, and getting rid of indentation. That may be true, but removing comments and indentation are too high a price to pay to speed up your code. I don't recommend it, and in any case, they are immaterial when you use a compiler.

There are better ways to get fast executing programs:

- Keep the number of files in a subdirectory reasonably small, that is, keep your subdirectory uncluttered. You don't have to put all your PRGs, DBFs, and NDXs

into one subdirectory. Indeed, most of the time you'd probably want them separated.

- Defragment your disk periodically so file sectors are located in contiguous areas of the disk and the software does not have to work so hard reading and writing data. You can use commercial defragmenters such as Disk Optimizer, Mace and Norton, or shareware programs like DOG, SST, and Desk Commando.

Removing  
comments and  
indentation are too  
high a price to pay  
to speed up your  
code.

- Use a disk cache. Note that Fox Software warns you that using a cache with FoxBASE+ 2.0 actually slows down the program.
- People tell you to eschew the LOCATE and CONTINUE commands in favor of the FIND and DO WHILE commands. It is still good advice. The latter need not read the whole database just to discover there are no more desired records to process. For the same reason, stay away from the SET FILTER TO command whenever you can. Although it is a very nice command because it saves you a lot of coding, it is inefficient. Behind the scenes, dBASE performs the slow LOCATE and CONTINUE commands when you say SET FILTER TO.

Well, that should give you some idea of the topics I'll explore in this column. I'll continue this discussion next time. §

*P. L. Olympia, Ph.D., is a scientist with a doctorate in Chemical Physics. He is better known as "Dr.*

*dBASE" and is coauthor of the book dBASE Power: Building and Using Programming Tools, soon to be published by Ashton-Tate.*

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by Keith Mund to be marketed  
by Ashton-Tate. Not yet released

# Creating Remote Workstations

One of the most common requests that we get is to connect remote workstations to a local area network (LAN). By definition, a LAN connects workstations, printers, and file servers in a relatively small geographic area. Usually, this area is a single building or a single campus. It is not always practical to keep all the LAN users within the geographic confines dictated by the selected LAN topology. Sometimes, users need to travel away from the confines of the LAN, but still communicate with other users of the network.

For example, a company that we work with in Denver uses a LAN for electronic mail. Company engineers travel to field sites around the United States. The engineers in the field use a modem with a Compaq portable computer to call up a modem on the LAN and, once the communication link is established, log on to the LAN.

There are essentially two ways that a remote workstation can connect to the LAN: (1) program execution occurs at the remote workstation or (2) program execution occurs at the LAN. The major difference be-

tween the two is where the program execution occurs.

## Execution at the Remote Workstation

Remote workstations can be connected to a LAN so that the programs to be executed will run in the remote workstation. To do this, a serial port is installed in a file server and is connected to an external modem via an RS-232 cable. Similarly, the remote workstation (PC) is configured with a serial port and an external modem. This connection is shown in Figure 1. Note that on some networks the serial port for the file server could be installed in a bridge workstation on the LAN.

The network operating system has to be set up to recognize the serial port in the file server for remote configuration. With Novell NetWare, this means running the AR-CONFIG.EXE program to configure NET\$OS.EXE.

In addition, a shell has to be created to run on the remote workstation. The shell will usually be configured with an ID string, baud rate, communication port, modem type, and a phone number to call. Generally, the shell will be put on a bootable disk that contains the system files and set up with an AUTOEXEC.BAT file to automatically invoke the shell.

Configuration of the network op-

erating system and the shell is not difficult, but a few tips will make it easier to maintain. First, write down the configuration choices you make. Second, as configuration parameters are often case-sensitive, always enter them the same way, such as all upper case, for both the network operating system and the shell.

Because of the speed of data transmission, the remote connection made in this manner will be considerably slower than a local workstation. Consider the case where a remote user has made the modem connection to the LAN. Now the user needs to log on to the network by executing the logon program. As execution of the logon program will occur at the remote workstation, the first thing that will happen is that the logon program will be "downloaded" or transferred from the file server to the remote workstation.

This is exactly what happens with a local workstation, except that the transfer speed between the file server and the local workstation is at 2.5 megabits per second (Mbps) (with Arcnet).

The transfer speed between the file server and the remote workstation is restricted to the speed of the modems, typically 2400 bits per second (bps). This means it can take several minutes just for the file transfer. Once downloaded, the program will execute at the speed of the local workstation which is relatively fast, but the next task to be executed will have to be downloaded from the file server to the remote workstation.

There are ways to get around this limitation. First, you can get faster modems, however experience has shown that the actual throughput of these modems is dependent upon the quality of the phone lines. Second, you can keep some of the executable files on the remote workstation so that only the data has to be downloaded. This requires a hard disk in the remote workstation.

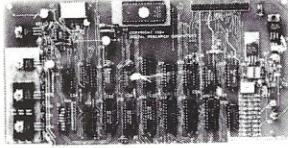
We have generally found this approach to be a less than satisfactory means to connect remote workstations. As a general rule, we connect remote workstations by allowing

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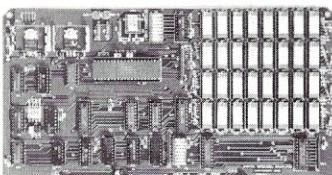
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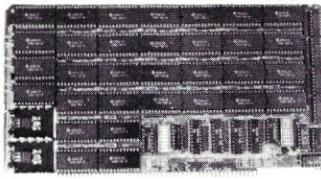
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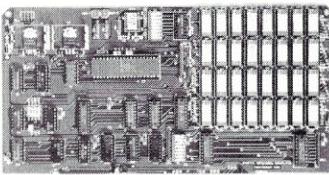
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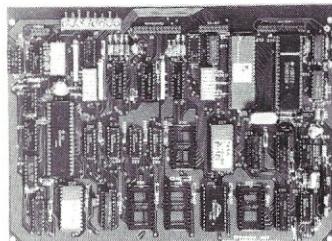
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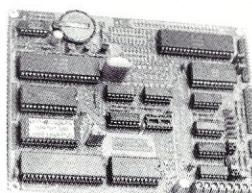
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execution of the programs that the remote workstation wants to use at the LAN. This approach will be discussed later.

### External Versus Internal Modems

In equipping remote workstations, we prefer external modems. An external modem has lights that can be readily observed. This is handy for troubleshooting communication problems since you can monitor the activity (for example, when the modem goes off hook). This is especially true when the remote user is not used to working with modems, and you have to troubleshoot problems over the phone. Further, it is often hard to hear the speaker of an internal modem once it is installed in a personal computer.

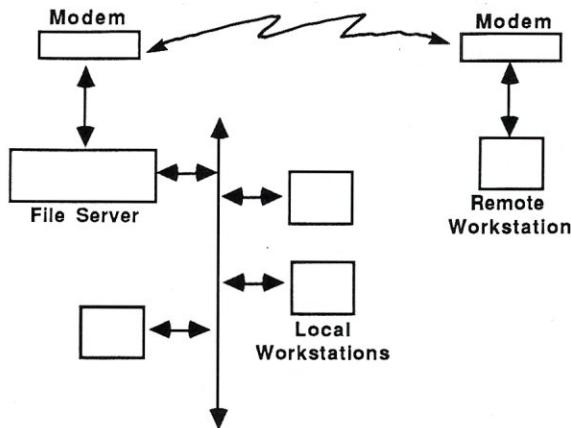
Note also that some 1200/2400-baud modems do not use the same method to handshake. Some modems use the CCITT V.22 standard and some use the Bell 2400 standard. The bottom line is that some modems will answer, but not "sync" up and make a connection. Some modems successfully handle both handshakes.

Our recommendation is to either use the same modem manufacturer at both the communication server and the remote workstation. An easy way out is to stick with Hayes and avoid the cheaper clones.

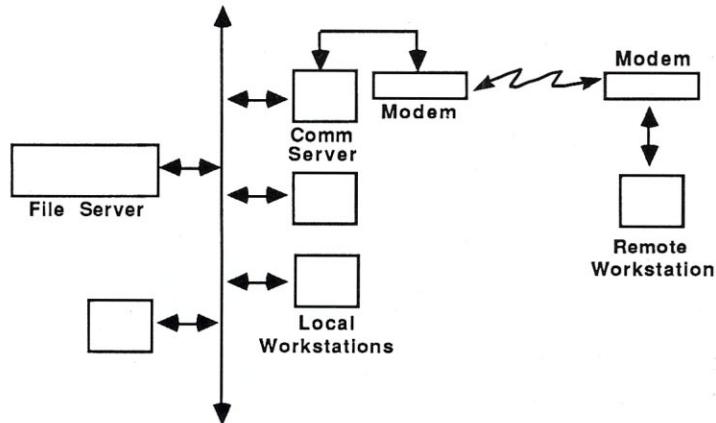
### Execution at the LAN

In the second method, a remote workstation executes the programs on the LAN, essentially "watching" the execution. For this to work, it is necessary to have a workstation on the LAN on which the remote workstation can run its program. This workstation, typically called a communications server or "comm server," will have a serial port, and an external modem connected by an RS-232 cable. The remote workstation (PC) will be set up as before, with a serial port and an external modem. This connection is shown in Figure 2.

The network operating system does not have to be changed for this remote configuration. The communi-



**Figure 1. Remote workstation runs programs downloaded from the host file server.**



**Figure 2. Remote workstation runs programs on a host workstation connected to the LAN.**



wasted workstation. The disadvantage is that the Chatterbox case is poorly constructed; the frame is easily bent and can be damaged in shipment, and the plug-in cards do not fit well.

The processor cards that install in the Chatterbox have switches on the back of them. Unfortunately, these switches interfere with the installation of the cards in the Chatterbox. Another disadvantage of the Chatterbox is that it is slow. J&L is working on a 286-based processor, and while this improves execution speed, the boards have the switches in even worse locations.

Here are some Chatterbox installation tips. Often, screwing the processor and network interface cards into the backplane of the Chatterbox causes the cards to slip out of the expansion slot of the motherboard. Unfortunately, leaving the cards loose can be equally troublesome. The basic problem is that the frame of the Chatterbox is too short, and the cards have to be bent to fit. Our remedy is to remove the motherboard, and install spacer washers under it. Slightly raising the motherboard will allow anchoring of the cards in the expansion slots.

To test the setup of the Chatterbox you can put a monitor card in with the processor cards and network interface card. This will let you watch the start up of the comm server. Our installers always take a monitor card with them, then when everything tests out correctly, they remove the card and close the Chatterbox.

It is important to note that the Chatterbox does not have any disk drives. It boots onto the network through the use of boot PROMs. The boot PROM installs on the network interface card, which permits the "diskless" workstation to boot itself and connect to the file server.

Boot PROMs are readily available for most network interface cards from the interface vendor. They are specific to both the network operating system and the network interface card, so do not assume that they are interchangeable. For example, a boot PROM for a 3Com Etherlink

card will probably not work with a Micom Interlan Ethernet card. And a Novell NetWare PROM for Arcnet is different from one for Ethernet or Token-ring. Check on the availability of boot PROMs when designing the network since not all LAN interface card manufacturers have them.

To work with boot PROMs on a Novell network it is necessary to run a program called DOSGEN. This creates a file called IBM\$DOS in the LOGIN directory. Instructions for DOSGEN are quite straightforward with one exception. It is necessary to have a formatted diskette for the process, and the diskette has to have the system file COMMAND.COM on it. When DOSGEN does not work, it is usually because the floppy disk used was not formatted with /S.

After working with several customers who wanted to promote LAN access to remote users, we have started to build our own comm server. The GS-2 communications server is custom built to the requirements of the customer, and has features such as multi-speed processors, attachable keyboards and monitors, as well as rack or desktop mountings. But key to our comm server is the ability to run a variety of communication processes in the comm server. For example, we can configure a comm server to allow remote users to dial in, as well as to house the Novell Asynchronous Communications Server (for dial in and dial out) and to provide a housing for gateways to IBM mainframes.

The Novell ACS is unique in that it allows dial-in and dial-out, and will be discussed in a future article, as will SDLC and X.25 gateways.

### Wrapping It Up

There are several questions that need to be asked when designing a connection scheme for remote users. For example:

- How often will users call in?
- How long will the average connection last?
- Will multiple modem speeds be required?
- Will remote workstations want

print capability?

- Will remote workstations want to perform file transfer?

The answers to these questions may affect the choice of the software to run in the comm server, but almost any option can be accommodated. One customer that we have in Denver even uses T1 phone links between the remote workstations and the comm server on the LAN. Another customer has a LAN with only one local workstation and all the other users attaching by means of comm server ports.

Regardless of the approach that you choose to use, the LAN does not have to be limited to locally attached workstations. Remote users can be connected to the LAN in a manner that will allow them to benefit from the same services to which LAN users have become accustomed. §

*B.J. Hall and Michael Cherry operate HallComm Network Services, a company devoted exclusively to designing and implementing LAN systems. HNS is located at 8101 East Prentice Ave., Ste. 304, Englewood, CO 80111; (303) 771-6387.*

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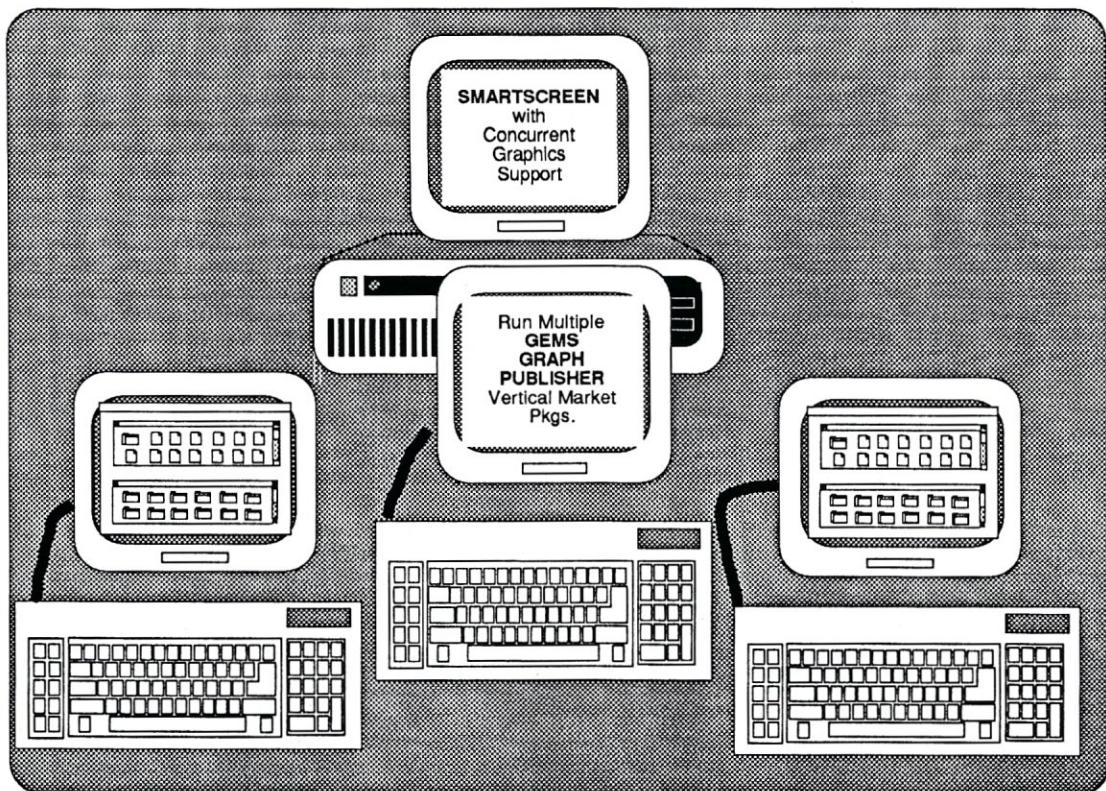
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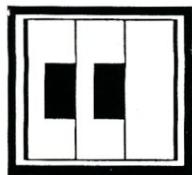
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# Number-Crunching Coprocessor Boards

**3** 86/387 machines and coprocessor boards are now becoming available, as is software that can run the 386 in both the 16-bit and the 32-bit protected modes, thereby breaking the 640-kilobyte (K) barrier.

I note in passing that human number crunchers should not be holding their breaths waiting for the availability of OS/2 to break the 640K barrier and open up the full potential of the 386 machine. It is necessary to distinguish between the two kinds of protected mode: 16-bit and 32-bit. The 16-bit mode will run on the 286 chip, and thus, by default, also on the 386 chip. The 32-bit mode will run only on the 386, but it will run quite a lot faster. OS/2 will only provide access to the 16-bit mode; thus it shortchanges the 386 user who really wants speed. It is rumored that a 32-bit protected mode version of OS/2 will not be available until 1989 at the very earliest.

Hence, we need to pay attention to the so-called DOS extenders, of which there are now several being offered. One important one comes from Phar Lap Software, which addresses only the 32-bit mode. I have just had a brief fling with another DOS extender from A.I. Architects, which provides versions for both the 16-bit and 32-bit modes, called DOS/286 and DOS/386, respectively. They also provide a 386/387 coprocessor board, called the HummingBoard, which is available in 16- and

20-MHz versions. I borrowed the 20-MHz version for a few days in order to run some tests on it.

## The HummingBoard

The HummingBoard comes with a lot of on-board RAM. My board had 6 megabytes (MB) of 256K chips, surface-mounted, standing on end, and taking up a fair chunk of real estate at the end of the board. I had no trouble at all installing the board, which connects into an 8-bit slot and so will fit into both XT's and AT's. You can only use a short card in the slot on the chip side of the board owing to the space required by the on-board RAM. In any case, you should run cool boards as neighbors. With megabit chips, this card will hold up to 24 MB. It is a true coprocessor board in that the 386 runs independently of the host CPU.

At the time I had it, this board was not quite ready to be used by the FORTRAN number-cruncher. By the time you read this column, there should be at least three 32-bit FORTRANs that can be used on it; including additions from MicroWay and one from Lahey. However, I was unable to prepare anything to run in the 32-bit protected mode on the board.

At the time I had the board, the only FORTRAN supported by A.I. Architects was Microsoft FORTRAN, version 4.0. Upon installation, you apply a few patches to the Microsoft libraries, then you can compile and link a program to get the usual .EXE file. This file can be run as is on the HummingBoard, which in this case is simply being compatible with an 8088. For example, you run program

XYZ on the board by typing HB XYZ. Assuming there is no XYZ.EXP file, the HB program will run XYZ.EXE. But you can then produce a relinked version of the program by submitting the .EXE program to be processed by the A.I. Architects' Express program. This produces a file with an EXP extension that takes precedence over .EXE programs for execution by the HB program in 16-bit protected mode.

Table 1 shows five floating-point intensive, benchmark programs that were run on several system configurations after compilation was done with Microsoft FORTRAN 4.0. In Table 1, S-whet and D-whet give single-precision and double-precision whetstones in kilowhetstones per second—standard benchmark programs. REMEZ is an IEEE digital signal-processing program that is floating-point intensive. SVD is a single-value decomposition program that operates on  $50 \times 50$  matrices. Roots finds complex roots of real polynomials. I used the Microsoft large model for compiling these programs. I also cut down the size of the largest arrays to reduce the size of one of the .EXE files so that I would not have to strip nearly all resident programs out of memory in order to run it. This means that the five programs executed faster than they would have if the huge model had been used.

## Performance

The direct execution in real mode of the .EXE programs on the HummingBoard was very impressive. In fact, it ran five times as fast as on my 9.54-MHz Number Smasher board, which itself runs about  $2\frac{1}{2}$  times faster than a standard XT.

The numbers in Table 1 for the .EXP files (i.e., running in 16-bit protected mode) were obtained for me by A.I. Architects from my .EXE files and run on one of their boards there. It shows that there is a significant loss of speed in going to 16-bit protected mode for these benchmark programs. This is the penalty that you pay for gaining the ability to break the 640K barrier. There is one

near exception to this statement in that the REMEZ program executed almost as fast in protected mode; I do not understand why this happened.

It is anticipated that there will be a significant gain in speed when one can go to the 32-bit protected mode. But the proof of that will have to wait for the arrival of 32-bit FORTRAN compilers used with a 32-bit DOS extender.

A 16-MHz HummingBoard with 2 MB onboard is \$2,895, and the 387 chip is another \$795. With 6 MB of RAM in 256K chips, the cost is \$4,695. With 24 MB of RAM in 1 megabit (Mb) chips on board, the cost is \$17,550. The 20-MHz versions of these boards cost \$4,295, \$6,095, and \$18,950, respectively, all without the 387.

### The Weitek 1167 Coprocessor Board

The next evolutionary step in the number-crunching revolution has just arrived. For about three years now I have been predicting that number-crunching speeds would see a big boost when some vendor put the Weitek 1164 and 1165 numeric coprocessor chips in PCs or on coprocessor boards because of the intrinsic speed of these chips. Weitek designed the 1167 coprocessor board to work with the Intel 386 chip. (The 1167 is a combination of the 1164 and 1165 chips, together with the 1163 80386 interface chip.)

New 386 machines are being announced every day, or so it seems. But there is one little item that determines the degree of their sophistication: whether or not they have a Weitek socket. In my view, which is certainly not free of bias, any 386 machine without the Weitek socket is

rather uninteresting. The Weitek socket has 121 pins in it, compared to 81 for a 387 socket, and is what the Weitek 1167 coprocessing daughter board plugs into. In turn, the 387 chip can be plugged into this daughter board. Thus, both numeric coprocessor chips are available to respond to their respective command sets.

MicroWay is acting as an OEM to Weitek to fit the 1167 daughter board to the 386 machines equipped with the Weitek socket. Because of the different geometries of these machines, it appears that a number of custom designs will be required. So far, I know of only the following 386 machines that have the Weitek socket, and they were all announced within the last few weeks: the Compaq 386/20, the new AT&T machines, the Tandy 4000, the Wyse 386 machine, and one from NCR. MicroWay has been doing its developmental work on the Tandy 4000, but apparently this is not an optimum machine because, according to Steve Fried at MicroWay, the 1167 is I/O bound in the Tandy 4000. Be warned that if you go out and ask the average salesman if any of these machines has a Weitek socket aboard, the response is likely to be, "A what?" Only Compaq has openly advertised its Weitek socket, and it is the only one of these companies that apparently plans to offer the Weitek coprocessor board to its customers.

MicroWay also expects to bring out a 386/387/1167 coprocessor board to plug into any AT compatible bus. Obviously, it will be best to use this in a 286 machine since you will have to replace the CPU chip anyway.

For nearly a year now I have been using the Weitek 1164 and 1165 chips as part of the optional floating

**Table 1. Benchmarks of HummingBoard (HB) plus some comparison computers.**

Computer	CPU	Speeds					Benchmarks				
		MHz	S-whet Kwhet/s	D-whet Kwhet/s	REMEZ sec	SVD sec	Roots sec				
PC/XT	4.77		89.53	80.0	25.0	183.0	12.0				
Number Smasher	9.54		194.9	168.4	11.53	76.26	6.26				
HB (real)	20.0		968.2	827.0	2.97	15.44	1.64				
HB (protected)	20.0		844.3	714.4	2.86	17.86	1.75				

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point accelerator in my Sun 3/260 workstation (see *Micro/Systems Journal*, May-June and September-October 1987). In this machine, the chips work with 25-MHz Motorola 68020 and 68881 chips and the result is an increase in the floating-point throughput by a factor of 2 to 4 (see the benchmarks in Tetewsky and Feenberg, *Micro/Systems Journal*, September-October 1987). The new Sun 4/260, to which I shall be upgrading later this winter, combines RISC chips with the Weitek chips on the CPU board, which are no longer optional, and achieves an additional factor of 2 in speed.

From various benchmarks, I have formed the impression that 16-MHz 386/387 chip combinations are roughly equivalent in performance to 25-MHz 68020/68881 chip combinations. Therefore, it is not surprising to see the following results published by Compaq about its internal benchmarks. Compaq quotes a Whetstone Index of 3.3 for the Sun 3/260 with

floating point accelerator (this evidently refers to millions of Whetstones per second or Mwhet/s for single-precision FORTRAN). The number I measure on my machine is 3.56 Mwhet/s. For the Sun 3/260 without the floating point accelerator, the company quotes 1.3 Mwhet/s, which agrees with my measurement of 1.26 Mwhet/s. For the 20-MHz Compaq Deskpro 386/20 without the 1167 coprocessor board, the quoted speed is 1.9 Mwhet/s. This illustrates the advantage of increased speed that Compaq gains with its new machine by using a 32K cache on the motherboard and various other tricks. For the Compaq machine running with the 1167 chip, the measure is 4.6 Mwhet/s, some 37 percent faster than the Sun 3/260.

One must be a little careful with these numbers because we are told very little about the operating systems and FORTRANs used to obtain these numbers. However, it is striking that the Compaq Deskpro 386/

20 is as fast as the fastest workstations presently available. I would expect the other 386 machines with Weitek sockets, even the 20-MHz machines, to run a little more slowly than this Compaq.

MicroWay will be selling its versions of the Weitek coprocessor daughter board for \$1,495. Compaq asks \$1,999 for its version.

### The Phar Lap DOS-Extender

In 1986, Phar Lap Software announced its 386 Software Development Series built around its 386 DOS-Extender. This is software that allows 32-bit, protected-mode applications to be run under the standard DOS operating system. Memory addresses are 32 bits wide in the protected mode, and so all available memory can be directly addressed. The purpose of the DOS-Extender is to give protected-mode programs full access to DOS services. For this to happen, the DOS-Extender must intercept all system calls and pass them to DOS in the real mode of the 386. It must also pass data into 386 real-address space, if necessary. It also allows applications to interface directly to I/O devices, to call ROM BIOS routines, and to access screen memory for instantaneous screen updates.

The development version of the 386 DOS-Extender requires you to call the DOS-Extender and pass to it the name of the protected mode program you want to run. However, the commercial application program developed under DOS-Extender will have a run-time version of DOS-Extender merged into a single .EXE file with the application, so that to the end user the application appears to be a natural part of the DOS environment. Language compilers are, of course, examples of such application programs.

In May 1987, Phar Lap Software announced that future versions of DOS-Extender would provide support for the Weitek WTL1167 Floating Point Coprocessor. When DOS-Extender is started, it will detect if an 1167 is present and, if so, it will enable a memory-mapped interface to this chip. If the chip is absent, a

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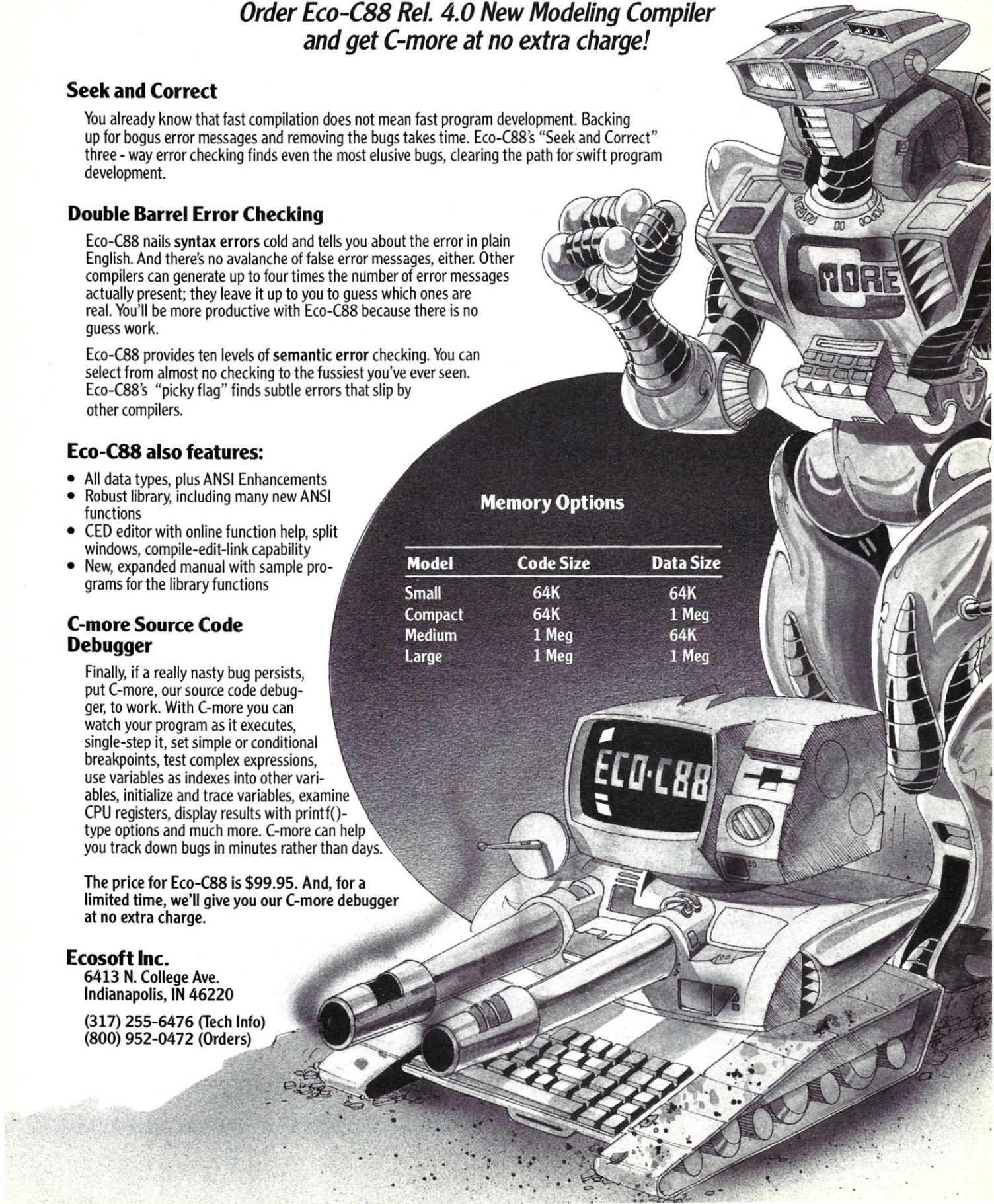
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# NEW PRODUCTS

*When contacting vendors, please mention that you read about their products in Micro/Systems.*

*Manufacturers who would like to have their products listed here should send their news releases to the Managing Editor, Micro/Systems Journal, 501 Galveston Drive, Redwood City, CA 94063.*

## New Software Products

### New Library for Turbo Pascal 4.0

Turbo Professional 4.0 is a library of more than 300 routines from Turbo Power for use with Borland's new Turbo Pascal 4.0. Included in the library are more than 30,000 lines of code optimized for Turbo Pascal 4.0, including pop-up resident routines, BCD arithmetic, long strings and large arrays, menus and fast windowing routines, EMS and extended memory access, and runtime error recovery. Sample programs that illustrate how the routines can be used include a memory-resident macro processor; a memory-resident programmer's quick reference chart; a memory-resident programmers calculator; an interactive menu maker that writes source code; and others.

Turbo Professional sells for \$99. For more information, contact Turbo Power, 3109 Scotts Valley Dr., Ste. 122, Scotts Valley, CA 95066; (408) 438-8608.

## PC-Compatible Hardware

### PS/2 Tape Backup Systems

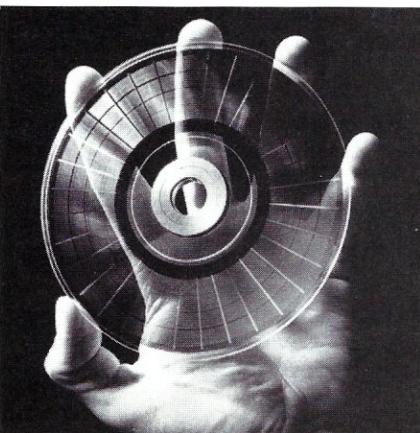
Emerald Systems Corporation has a new series of six tape backup subsystems for the IBM PS/2 Models 50, 60, and 80. They can be used in standalone or networked workstations, including DOS and Novell NetWare environments. The 1/4-inch tape backup products range in capac-

ity from 60-150 megabytes. All of Emerald's PS/2-compatible products include Emerald Systems' ASP backup software utility, which permits total control over the backup process, including selected file backup, password control, unattended backup, and advanced restore facilities.

For more information about this new series of PS/2 backup products, contact Emerald Systems Corp., 4757 Morena Blvd., San Diego, CA 92117; (619) 270-1994.

### ISi WORM System Software is Compatible to DOS

Information Storage Inc. (ISi) has new software for its optical WORM (Write Once, Read Many times) drive subsystems. WORM-TOS (Transparent Optical Software) is compatible with DOS yet transparent to applications and utilities. WORM-TOS supports all DOS features, including subdirectory trees; renaming, deleting, or appending files; and selective file alteration. It allows direct access to the optical disc using standard DOS commands and without a mount command. WORM-TOS also allows the



user to trace files and subdirectories backward through previous versions.

ISi's optical drive subsystem is ideal for extending the capacity of a system's hard disk drives while providing on-line backup capability. It can also provide savings to users who have a need for high-capacity information storage. ISi WORM drives

use 5 1/4-inch Certified Optical Storage Media; removable optical disk cartridges that come in 115-megabyte (MB) and 230 MB formats, which sell for \$100 and \$125, respectively. Since there are no magnetic components to these media, they are safe to use in the presence of strong magnetic fields.

An ISi 525 WC Optical Disc Subsystem for internal mount in an IBM PC, PC/XT, PC/AT, or compatible is available for \$2,595, including WORM-TOS software. An external unit with powered cabinet, drive, controller card, and software is available for \$2,795. For more information about ISi's WORM-TOS, contact Information Storage Inc., 27687 Janitell Rd., Colorado Springs, CO 80906; (303) 579-0460

## Other Hardware Products

### Modem With Mind of Its Own

The AJ 9631-SA is Anderson Jacobson's new V.32 modem offering full duplex, 9600 bps communication on dial-up networks or on 2/4-wire leased lines. The new modem is fully V.32 compatible and provides Trellis coded modulation, local and remote echo cancellation, and satellite transmission capability. In leased-line operation, the AJ 9631-SA features Unattended Automatic Dial Back Up (UADBU). User-selected Trellis coded modulation adds signal redundancy for enhanced error control, and local and remote echo cancellation and automatic adaptive equalization preserve data transmission quality. The AJ 9631-SA also features a V.25 bis auto dial for both synchronous and asynchronous dialing. On the switched network in leased line operation, the mode provides single call Unattended Dial Back Up (UADBU), and should the leased line fail, the unit dials a prestored number to reestablish a dial network connection.

The AJ 9631-SA sells for \$3,095. For more information, contact Anderson Jacobson, 21 Charcot Ave., San Jose, CA 95131; (408) 435-8520.

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Starting with the January issue, *Micro/Systems Journal* will be providing technical articles, columns, and reviews to computer system integrators every month. We are seeking new authors with innovative ideas and system applications that can be shared with other professionals. For example, over the next few months we plan to offer articles about:

- *Interfacing to the OS/2*
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- *PC Multiuser Operating Systems*
- *386 Software Development Tools*
- *UNIX on the PC*

We would welcome your contributions on any of these subjects. Please contact:

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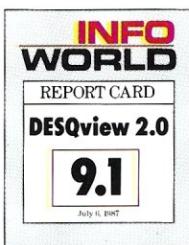
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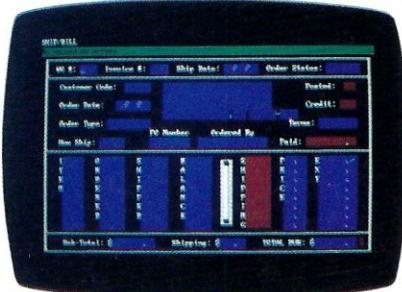
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